GEORGIA TECH GT–VDAG
VLSI DESIGN VERIFICATION DOCUMENT

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Georgia Institute of Technology
Atlanta, Georgia 30332–0540

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INTRODUCTION

There are eleven (11) Georgia Tech VLSI designs (see Table 1) in the AHAT Program. Each of these designs has been produced by Georgia Tech using the Genesil Silicon Compiler. Each design has passed the design verification process at Silicon Compiler Systems / Mentor Graphics and each has been fabricated in a bulk CMOS process (fabrication of certain chips was not complete when this document was released). Each of the Georgia Tech designs listed in Table 1 is being delivered to USASDC and to the Harris Corporation for conversion and fabrication in a rad–hard process. The program under which this work is done is AHAT (Advanced Hardened Avionics Technology). This document includes design information for the Georgia Tech data address generation chip, GT–VDAG.

Table 1. Georgia Tech Chip Set for AHAT

Design	DV Passed	Tape Delivered	Fabricated	Tested
GT–VFPU/1A	1/17/89	8/3/90	5/19/89	4/4/90
GT–VNUC				
GT–VTF				
GT–VTHR	12/11/90	2/15/91		
GT–VCLS	1/26/90	7/12/90	7/13/90	
GT–VCTR	2/8/90	7/12/90	7/13/90	
GT–VIAG				
GT–VDAG	2/22/91	2/25/91		
GT–VSNI	1/17/89	5/23/90	4/14/89	4/4/90
GT–VSM8	1/17/89	6/8/90	5/6/89	4/4/90
GT–VSF	9/12/89	7/19/90	7/13/90	

GT–VDAG : Data Address Generation Chip

1. Design Verification Checklist

The DV checklist attached in Appendix A.

2. Functional Description

This section describes briefly the function of the chip and the modules at core level.

2.1. Module adr_ptr_mod

This module maintains the adress pointer and address pointer limit. The address pointer may be loaded externally (if so, the task pointer is automatically added in), or it may be changed by an increment or decrement instruction. The amount to increment or decrement may come from data memory (via the f_r_1_as bus) or instruciton memory (via s_off). Because the increment/decrement instruction is executed immediately, the module contains a restorable DFF which can be restored in the event of a flush. "adr_ptr" is used by the address generators in certain addressing modes, "adr_ptr_lim" is used by the address generators for range checking, and "ap_apl" is used to examine the contents of either adr_ptr or adr_ptr_lim.

2.2. Module boot_ctrl

This module produces outputs that are driven onto the internal control lines "rs_off[11:0]" as well as r, s, and f_adr_mod[3:0]. It is used during booting (booting = 1) to control the DAG chip in parallel with the IAG boot controller. Thus, DAG can execute a simple loading program when first powered up.

2.3. Module decoders

This module decodes load instructions and checks for attempts to execute kernel instructions in the user mode. (Store instructions are decoded in various modules as needed.) Note that all instructions are delayed one cycle in this module except for incr_ap and decr_ap. Instruction cancelling is initiated by reset and flush conditions. Freeze cancelling is handled by individual modules.

2.4. Module error_mod

If the r, s or f addresses exceed their limits, it sets a corresponding RS flip–flop in the "error_ff" module. The proper ranges depend on the addressing mode, and range checking is only carried out in the user mode (kernel_mode = 0). Other modules check for a non–zero error condition and provide addtional control logic.

2.5. Module f_adr_gen

This is one of three almost identical modules which generate the three data addresses used by data memory and the ALU. R and S are data memory read addresses and F is the data memory write address.

The address calculations are performed in a datapath named "super_dp". Most of the control logic is found in a logic–compiled module named "super_ctrl". Time–critical control logic (which is the remainder of the control logic) is found in a random logic block named "critical_rl".

The "super_dp" supports the following features. There is an index register that can be added in to form the final address (depending on the addressing mode). It can be loaded from the data bus, the "s_offset" instruction field, or the post–index adder, and loading is controlled in "idx_ctrl". The operation performed on the index after it is used is controlled by the post index operation stored in a register in "post_idx_ctrl". A base address can be used in place of that specified in the instruction. (The addressing mode determines whether the instruction or the base register is used.) Loading it is controlled in "base_ctrl". Finally, the index (if used) is added to either the base register or the instruction field, and this value is added either to the task pointer or the address pointer. This produces the address, which in the case of the f_adr_gen is the f address. Internal registers, such as the base register and index register, can be read out. Range checking is performed in the user mode. Additional logic permits overflows to be reset, flushed, or frozen.

2.6. Module r_adr_gen

This module is essentially identical to the f_adr_gen. The R address is a data memory read address, and the R bus can contain data from data memory or from any input device.

2.7. Module s_adr_gen

This module is essentially identical to the f_adr_gen. The only significant difference is that the selection of whether to use the boot instruction or the external instruction is made inside this module. (In the case of R and F address generators, this is carried out in rf_off_mode_mod.

2.8. Module fr1as_mod

This module controls the f_r_1_as bus. This bus is used to load the registers. If r_adr_mode is 3, the value to be loaded is in instruction memory, and so the bus is driven by s_offset. Otherwise, it is driven by the RF bus. Depending on the values of the operand dependency check bits, the bus takes on the value of R delayed by one cycle, F delayed by one cycle, or F without delay. When booting, the bus is forced to R delayed by one cycle.

2.9. Module inst_reg_mod

This module performs reading and writing of instruction memory. To read instruction memory, the registers are loaded from the instruction fields and read out over the RF bus in two separate operations. To write instruction memory, the registers are loaded from the f_r_1_as bus (i.e. like any other internal register) and then the instruction bus is enabled as an output bus, the value being driven by the registers.

There are two registers, numbered 2 and 3. Registers 0 and 1 are on the IAG chip. Register 2 is used for RF offsets and adress modes. Register 3 is used for S offsets and address modes.

2.10. Module odc_rf_mod

This module performs operand dependency checking and multiplexes R and F address and S and F address. Operand dependency checking is a means of tracking in hardware the status of intermediate results in the ALU. If an operand is needed but has not been written to data memory from the ALU, the internal feedback paths of the ALU can be used anyway. Thus, variables can be accessed and used in calculations before their values are written out. The operand dependency values can be overridden by a special instruction, and they are forced to zero during booting.

2.11. Module r_out_mod

This module is used to read out internal registers. It is a series of multiplexers, and it drives the R bus.

2.12. Module rf_off_mode_mod

This module multiplexes either the RF instructions or the boot rom instructions onto the internal RF instruction bus. This bus is used in turn by the R and F address generators.

2.13. Module rs_mux_mod

This module controls whether the internal instruction bus "rs_off" is driven by r offset or s offset. All DAG load instruction can load values into registers either as constants, which come from "s_offset" in instruction memory, or as variables, which come from data memory via the RF bus. For constant loading, the instruction is specifed by r_adr_mode=3 and the rs_off bus is driven by r_offset. For variable loading, the instruction is specified by s_adr_mode =3, and the rs_off bus is driven by s_offset.

2.14. Module task_ptr_mod

This module contains the task pointer and task pointer limit registers. All addresses in user mode programs have a "task pointer" added in to thier value. This permits multiple user programs to be active in memory at once. The task pointer limit is the upper limit of the current user program's data area. Thus, it is used for range checking.

3. Signal Descriptions

3.1. Inputs

A description of the inputs and outputs to the DAG are described below. All signals are active high except those that start with "N_".

Name	Timing	From	Purpose
Booting	VB(t)	IAG	Puts DAG in booting mode
Guard	VB(t)	IAG	Disables loading of new instructions
Clk	Clock	Ext.	System clock
DAG_R_en	VB(t)	IAG	Enables RF bus output drivers
Flush	VB(t)	IAG	Cancels current and previous instructions
Freeze	VB(t)	IAG	Suspends execution
Ids_eq_ods_1	VB(t)	IAG	I/O device consistency check
Ids_eq_ods_2	VB(t)	IAG	I/O device consistency check
Ids_freeze	VB(t)	IAG	Determines whether in input or output mode
Inst_en	VB(t)	IAG	Enables instruction output drivers
Kernel_mode	VB(t)	IAG	Determines whether in kernel or user mode
Inst_rd	VB(t)	IAG	Enables loading of instruction registers
N_reset	VB(t)	IAG	Resets the system
Ods_freeze	VA(t)	IAG	Determines whether in input or output mode
Pc[3:0]	VB(t)	IAG	Specifies boot instruction
Valid_intr	VB(t)	IAG	Indicates interrupt condition; cancels current instruction

3.2. Outputs

The primary destination is listed below. There are other "destinations" that are not listed. All signals are active high except those that start with "N_".

Name	Timing	To	Purpose
DAG_Error	SB(t)	IAG	Flags an error condition
R_eq_f_2	VB(t)	FPU	Operand dependency checking
R_eq_f_1	VB(t)	FPU	Operand dependency checking
RF_adr[25:0]	W(t)	DataMem	Read/Write address
S_eq_f_1	VB(t)	FPU	Operand dependency checking
S_eq_f_2	VB(t)	FPU	Operand dependency checking
SF_adr[25:0]]	W(t)	DataMem	Read/Write address

3.3. Input/output

These are tri–stated I/O signals. All signals are active high except those that start with "N_".

Name	Timing	From/To	Purpose
RF[31:0]	W(t)	I/O	General system read/write bus. Driven by data mem, fpu, and I/O.
RF_adr_mode[3:0]	VB(t)	InstMem	R and F address instructions
RF_off[25:0]]	VB(t)	InstMem	R and F address instructions
S_adr_mode[3:0]	VB(t)	InstMem	S address instructions
S_off[25:0]]	VB(t)	InstMem	S address instructions

4. Final Notes

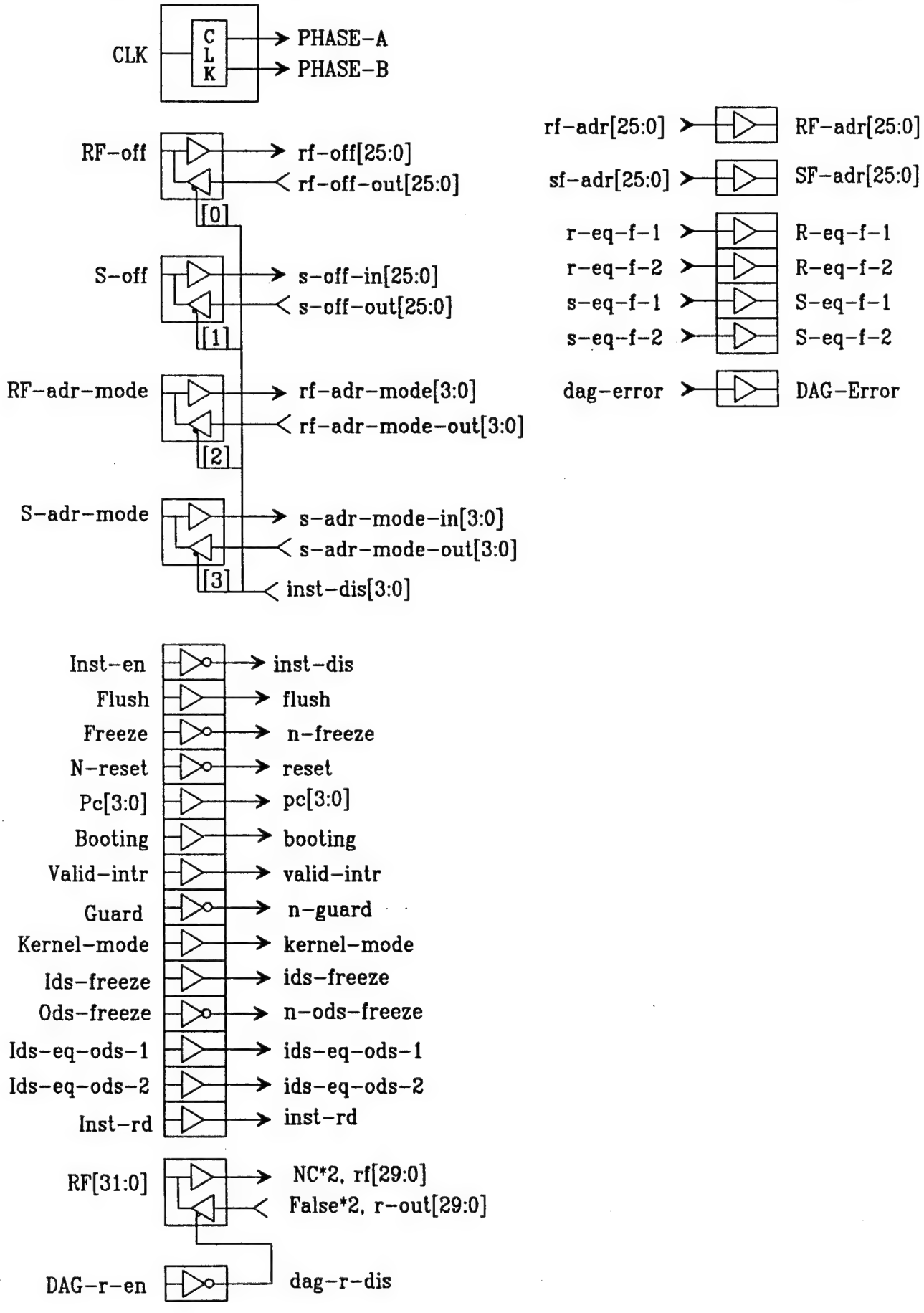
The recompile as part of DV changed the size of DAG slightly (about 2 mils on a side), and timing was not affected substantially. The bonding wire lengths and angles were not approved by Genesil's Padring CCC, but HP has approved it for prototype fabrication.

The DV tape contains a file named "dag.tar.Z". This file is about 28MB in size, and the database, when uncompressed, is about 120 MB. To restore it, do the following.

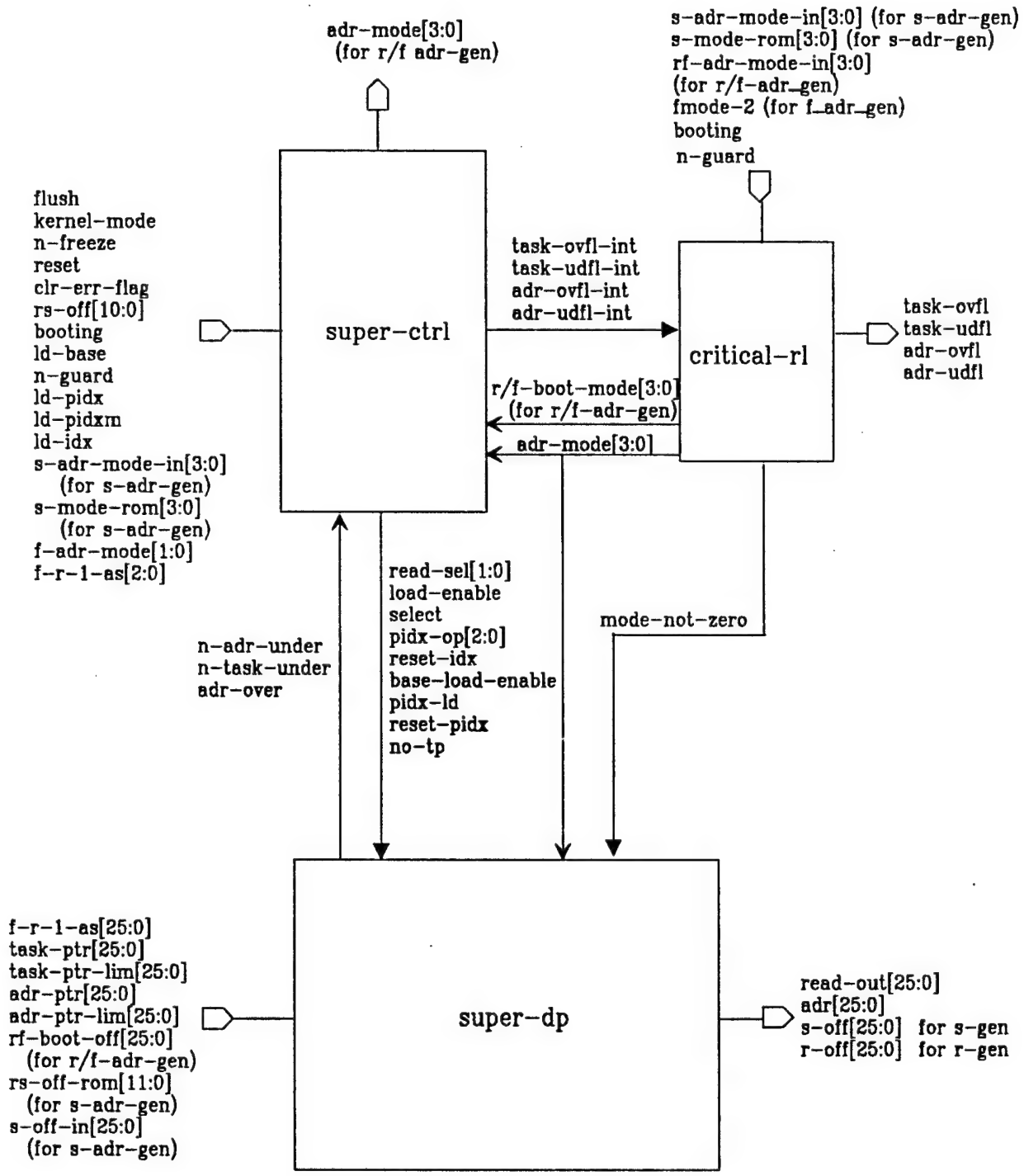
1. Go to the location on the destination machine and destination directory and execute "tar xv".
2. After dag.tar.Z has been extracted, type "zcat dag.tar.Z | tar xvf –".

5. Block Diagrams and Schematics

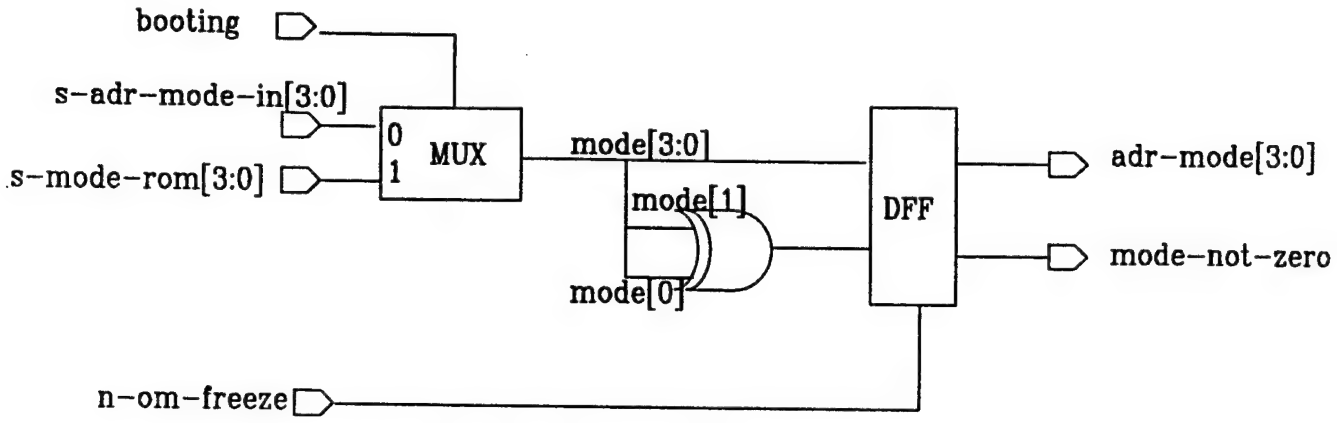
Diagrams showing how DAG is connected into the GT–EP chipset can be found in the list of schematics for GT–VIAG. Included below is a set of drawings for GT–VDAG itself.


CLK
C
L
K
PHASE-A
PHASE-B
RF-off
rf-off[25:0]
rf-off-out[25:0]
[0]
S-off
s-off-in[25:0]
s-off-out[25:0]
[1]
RF-adr-mode
rf-adr-mode[3:0]
rf-adr-mode-out[3:0]
[2]
S-adr-mode
s-adr-mode-in[3:0]
s-adr-mode-out[3:0]
[3]
inst-dis[3:0]
rf-adr[25:0]
RF-adr[25:0]
sf-adr[25:0]
SF-adr[25:0]
r-eq-f-1
R-eq-f-1
r-eq-f-2
R-eq-f-2
s-eq-f-1
S-eq-f-1
s-eq-f-2
S-eq-f-2
dag-error
DAG-Error
Inst-en
inst-dis
Flush
flush
Freeze
n-freeze
N-reset
reset
Pc[3:0]
pc[3:0]
Booting
booting
Valid-intr
valid-intr
Guard
n-guard
Kernel-mode
kernel-mode
Ids-freeze
ids-freeze
Ods-freeze
n-ods-freeze
Ids-eq-ods-1
ids-eq-ods-1
Ids-eq-ods-2
ids-eq-ods-2
Inst-rd
inst-rd
RF[31:0]
NC*2, rf[29:0]
False*2, r-out[29:0]
DAG-r-en
dag-r-dis

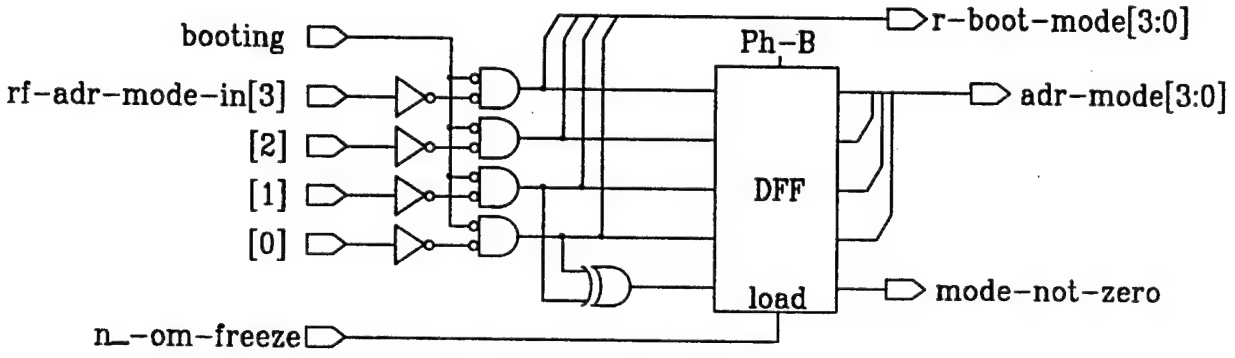
I/O Signals


adr–mode[3:0]
(for r/f adr–gen)
s–adr–mode–in[3:0] (for s–adr–gen)
s–mode–rom[3:0] (for s–adr–gen)
rf–adr–mode–in[3:0]
(for r/f–adr_gen)
fmode–2 (for f_adr_gen)
booting
n–guard
flush
kernel–mode
n–freeze
reset
clr–err–flag
rs–off[10:0]
booting
ld–base
n–guard
ld–pidx
ld–pidxm
ld–idx
s–adr–mode–in[3:0]
(for s–adr–gen)
s–mode–rom[3:0]
(for s–adr–gen)
f–adr–mode[1:0]
f–r–1–as[2:0]
super–ctrl
task–ovfl–int
task–udfl–int
adr–ovfl–int
adr–udfl–int
critical–rl
task–ovfl
task–udfl
adr–ovfl
adr–udfl
r/f–boot–mode[3:0]
(for r/f–adr–gen)
adr–mode[3:0]
read–sel[1:0]
load–enable
select
pidx–op[2:0]
reset–idx
base–load–enable
pidx–ld
reset–pidx
no–tp
n–adr–under
n–task–under
adr–over
mode–not–zero
f–r–1–as[25:0]
task–ptr[25:0]
task–ptr–lim[25:0]
adr–ptr[25:0]
adr–ptr–lim[25:0]
rf–boot–off[25:0]
(for r/f–adr–gen)
rs–off–rom[11:0]
(for s–adr–gen)
s–off–in[25:0]
(for s–adr–gen)
super–dp
read–out[25:0]
adr[25:0]
s–off[25:0] for s–gen
r–off[25:0] for r–gen

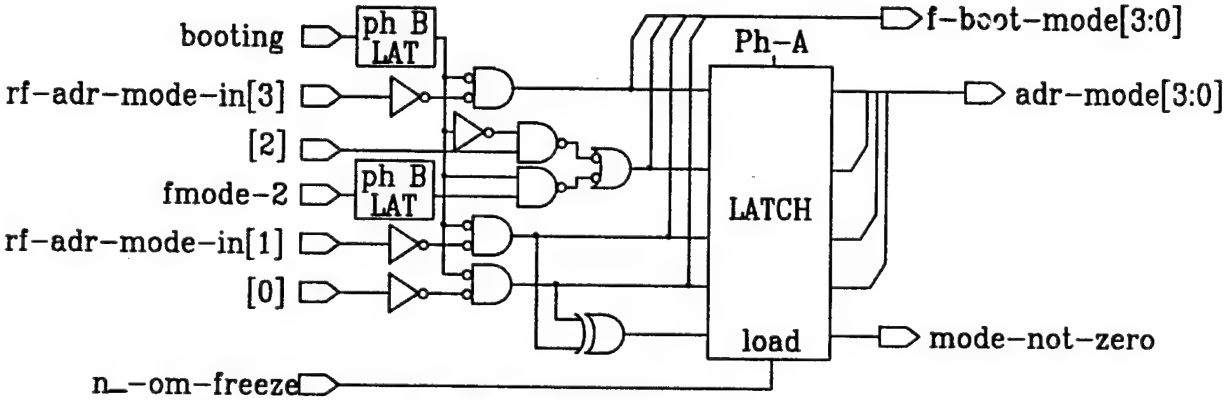
r/s/f–adr–gen



s-adr-gen/critical-rl

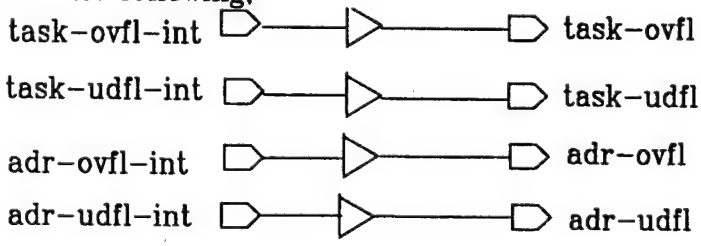


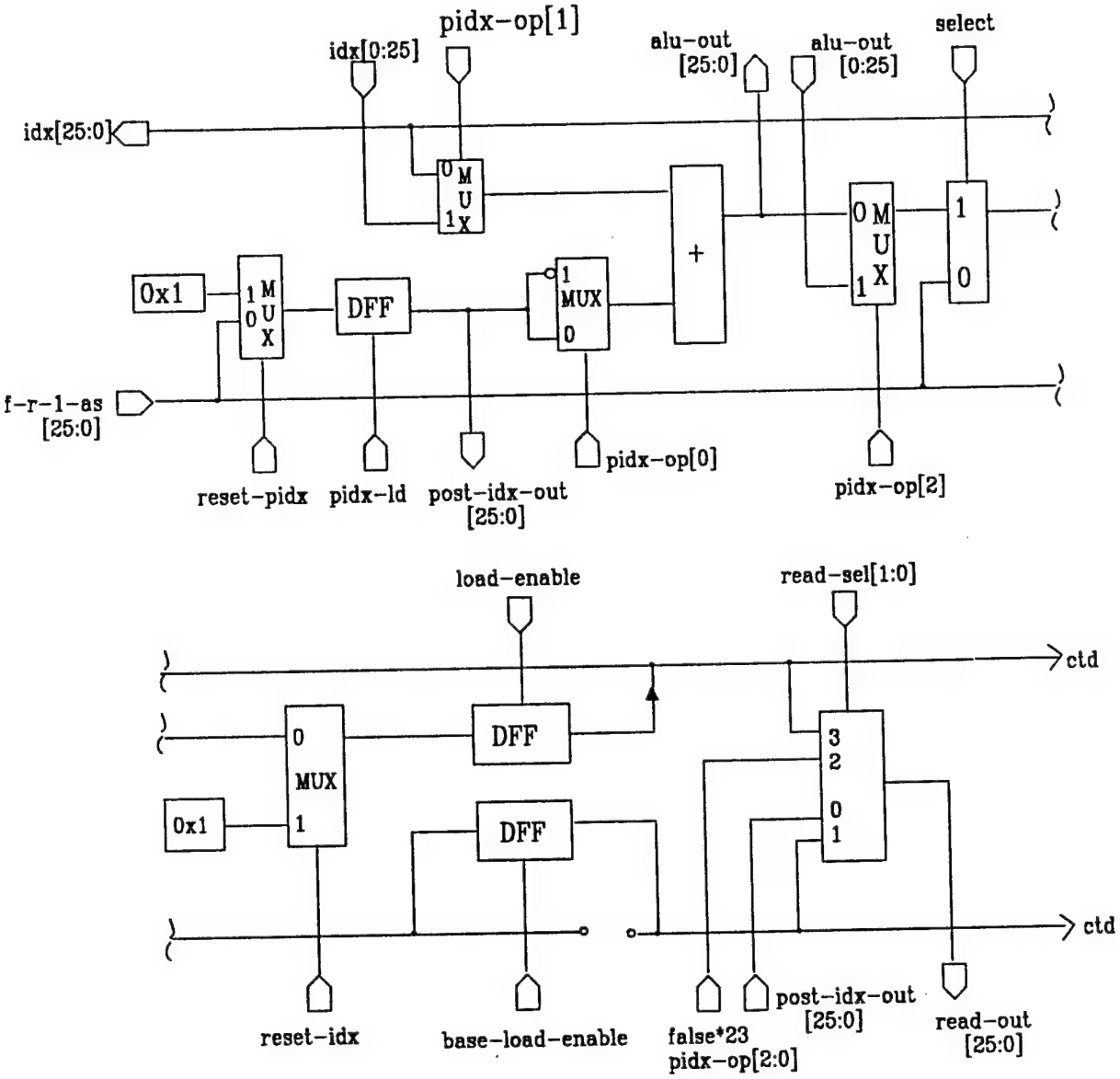
r-adr-gen/critical-rl



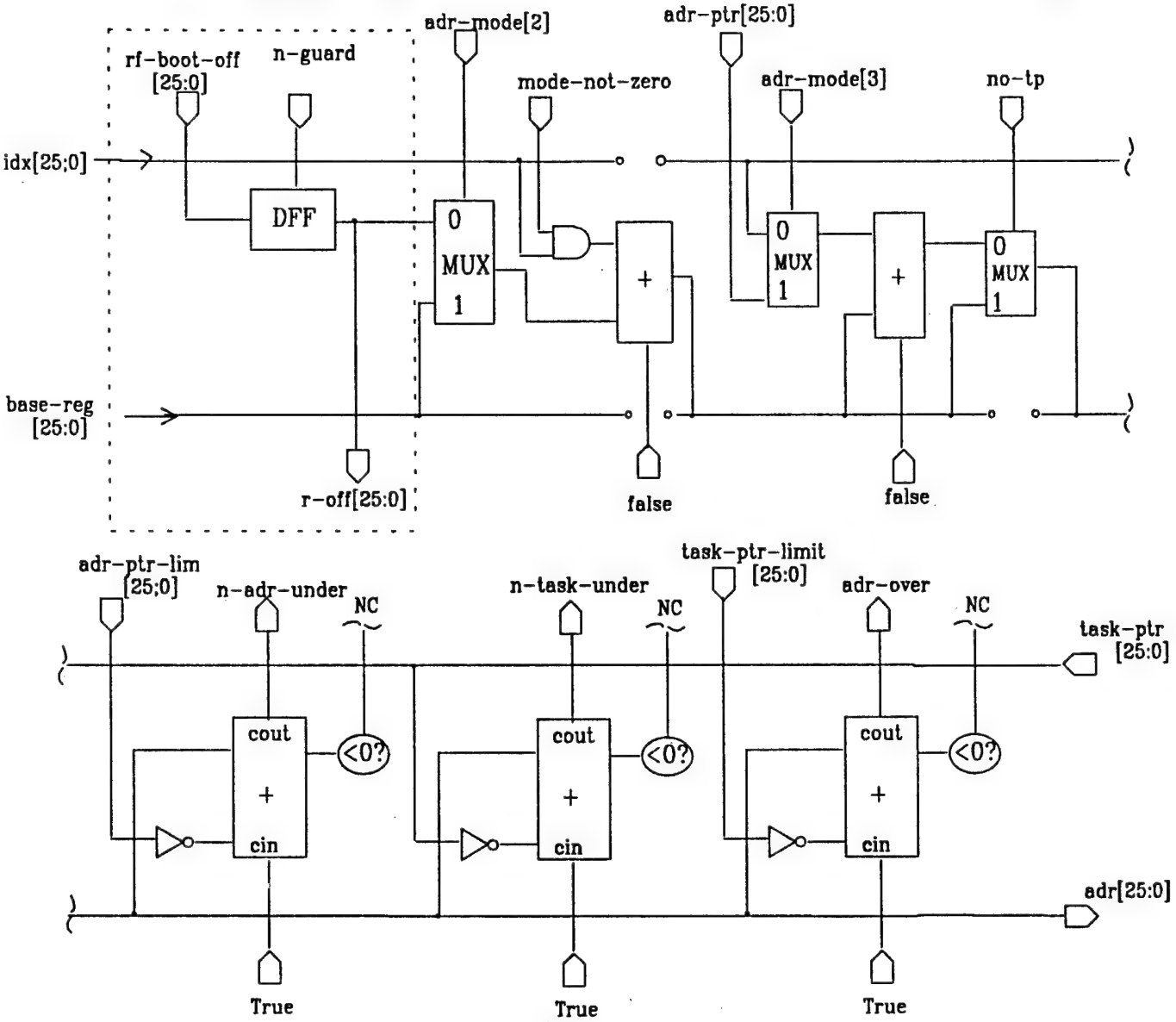
f-adr-gen/critical-rl

All adr-gen datapaths have been combined into one datapath named "super-dp".
All adr-gen random logic blocks have been placed into a module named "super-ctrl" which is logic compiled.
The logic shown here has been removed from super-ctrl and placed into a random logic block named "critical-rl".
All have the following,

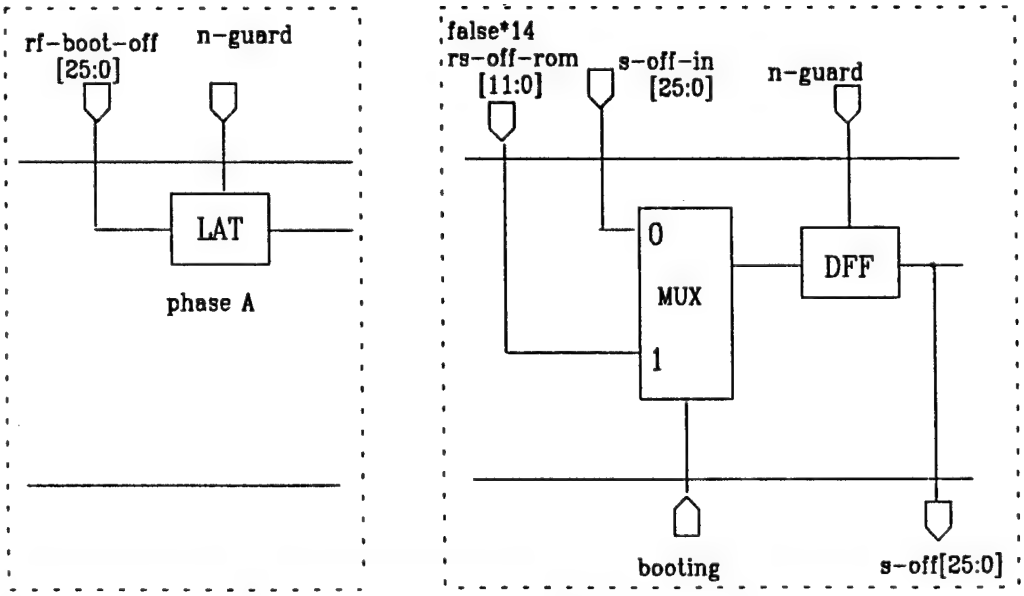




Netlist change	
DAG	adr–gen
n–guard	n–om–freeze

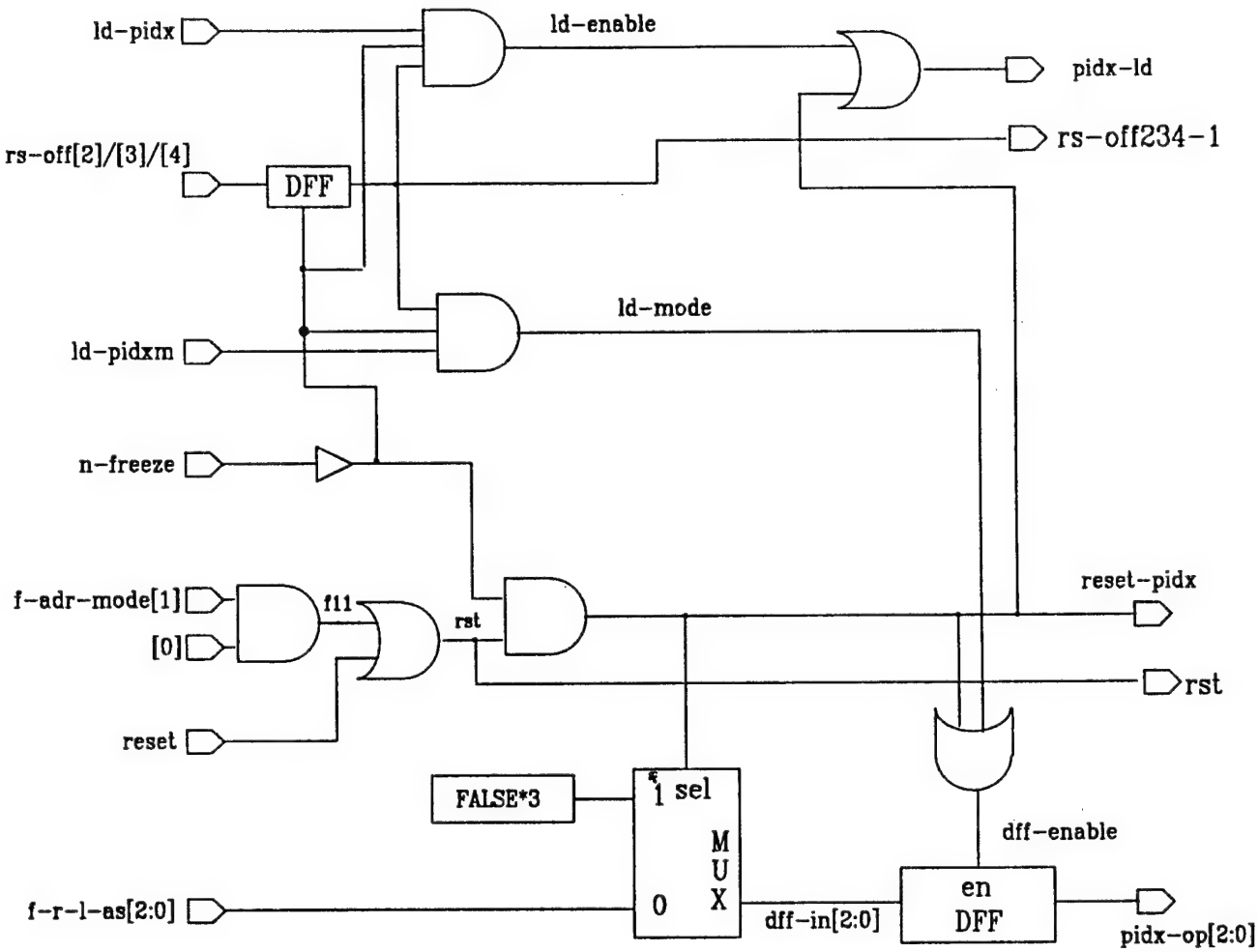


r-adr-gen/super-dp



modification for
f-adr-gen/super-dp

modification for
s-adr-gen/super-dp



pidx–op	"1" means	"0" means
[2] [1] [0]	bit–reverse adder output bit–reverse index input subtract post–idx–reg	leave adder result intact leave index input intact add post–idx–reg

Default

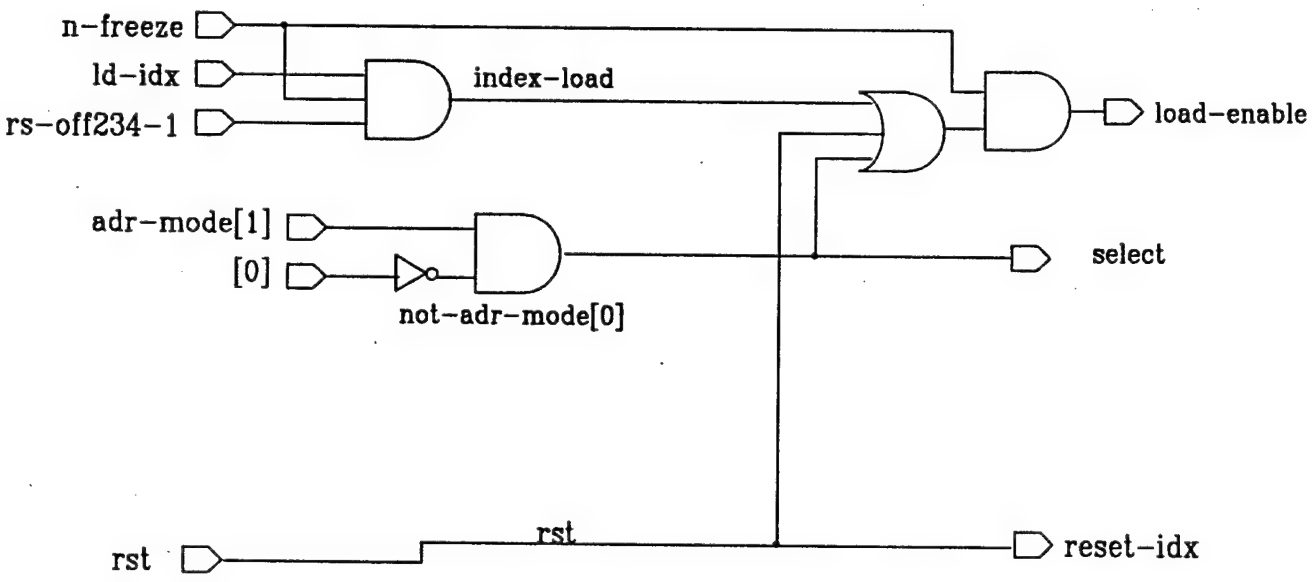
[2]	[1]	[0]
0	0	0

super–ctrl/post–idx–ctrl

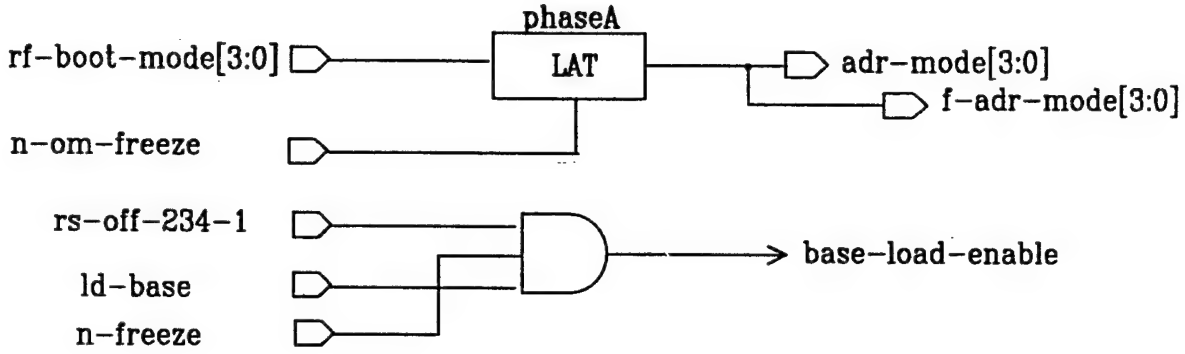
CONDITION

ld-idx=1
rs-off[2/3/4]=1 } = LOAD-EN

LOAD-EN	load f-r-l-as
adr-mode[1:0]=10	load idx-in
reset or f=adr-mode=11	load "0x1"
anything else	don't load



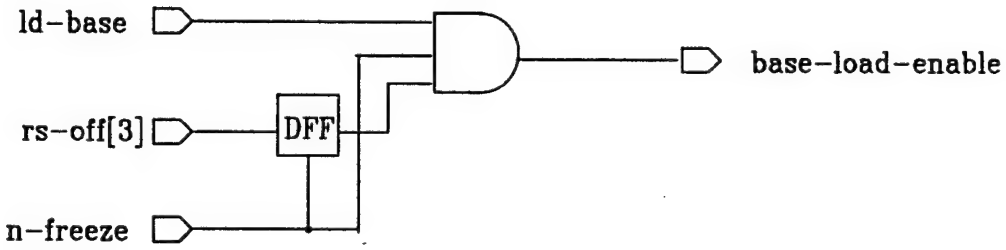
super-ctrl/idx-ctrl

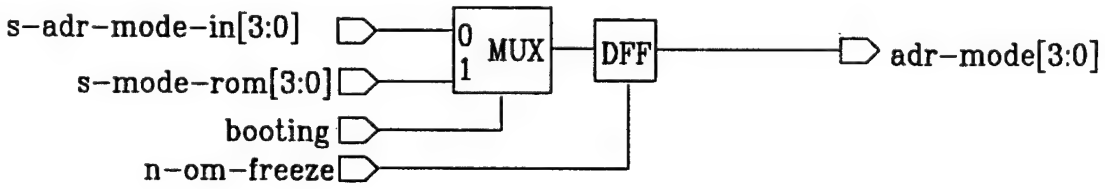


f-adr-gen/base-ctrl

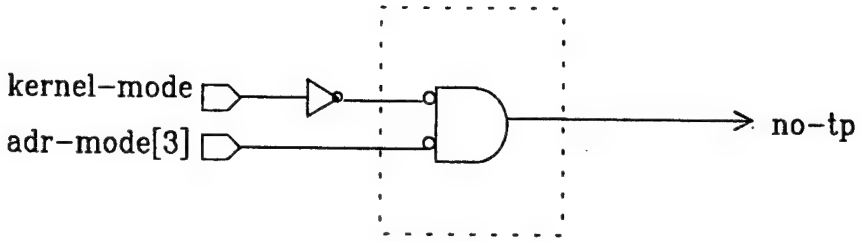
NOTES: f-off[25:0] is not connected.
r-adr-gen is idendical except.

f-adr-gen	r-adr-gen
phase A latch	phase B DFF's
rs-off[4]	rs-off[2]
f-off[25:0]	r-off[25:0]
↓	↓
NC*26	NC*14,r-off[11:0]
f-adr-mode[3:0]	r-adr-mode[3:0]

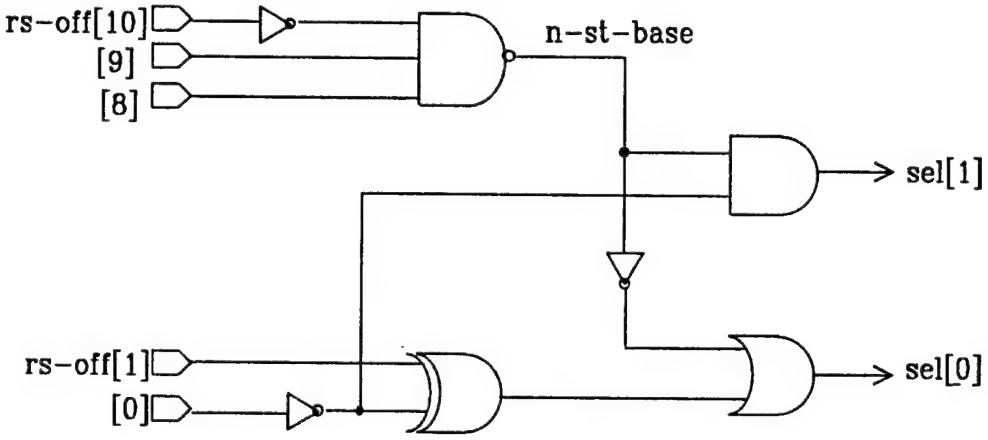




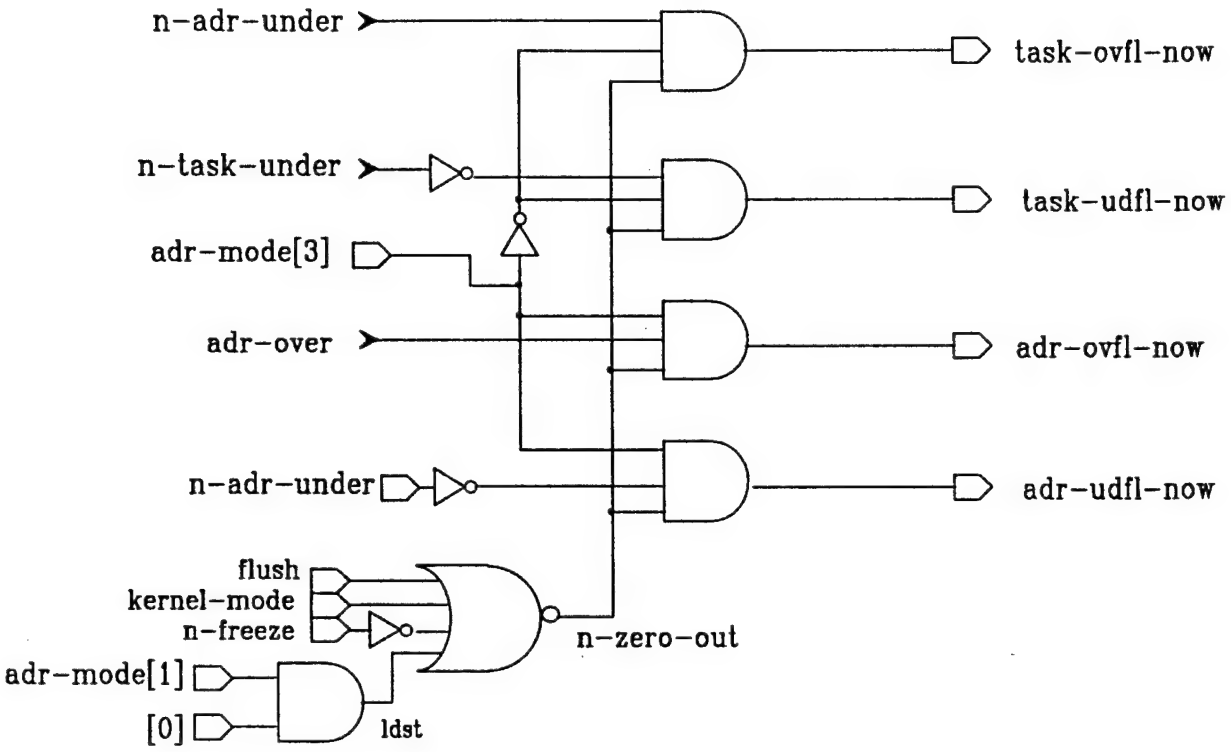
s-adr-gen/base-ctrl



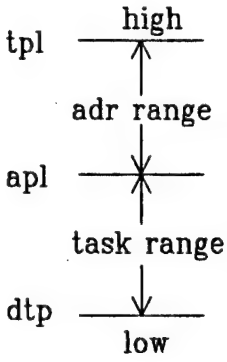
super–ctrl/adr–gen–dp–ctrl



super–ctrl/read–mux–ctrl

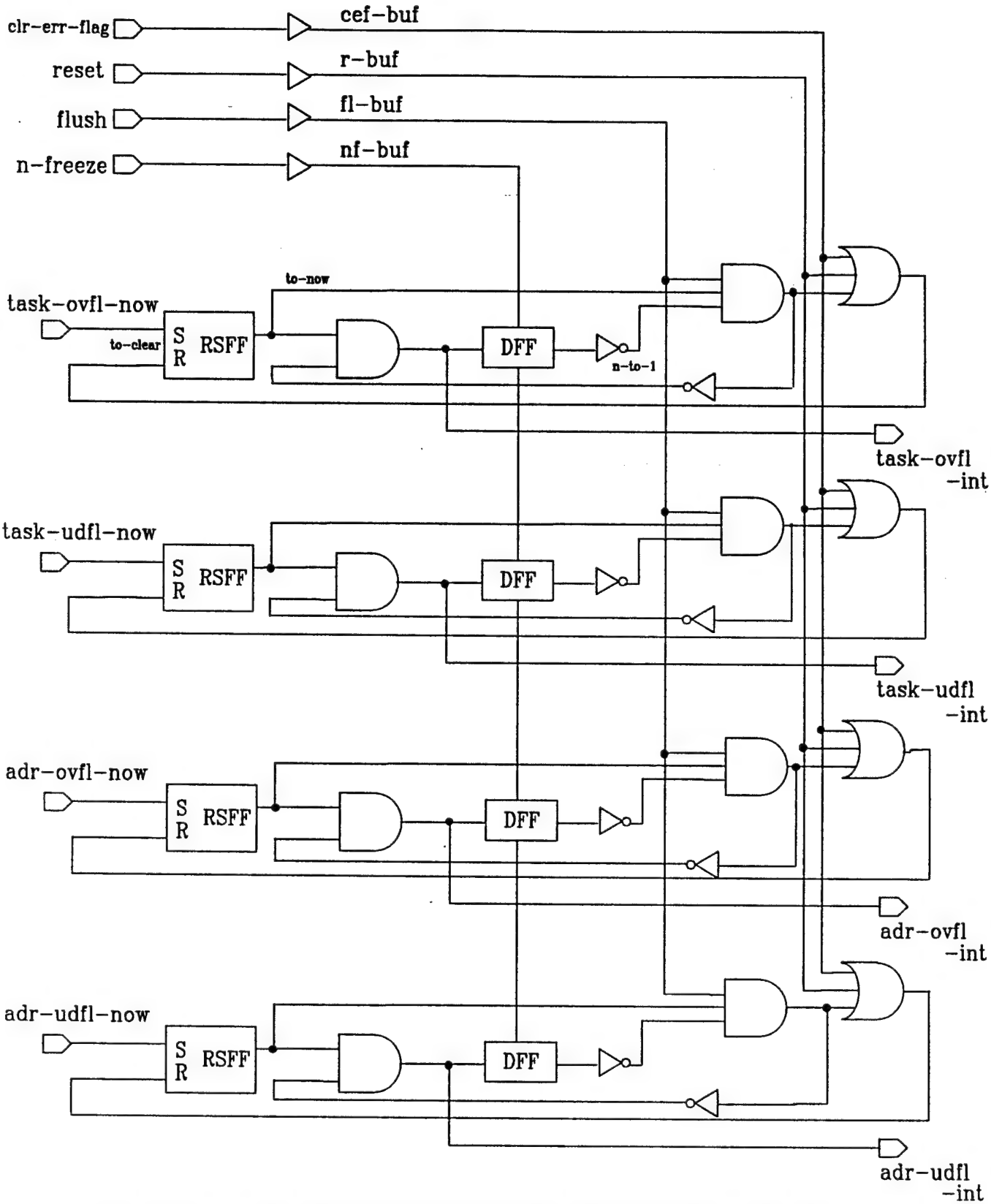


super–ctrl/over–under–ctrl



This is the address range associated with each task. Local variables are accessed by the address pointer and must be located between the apl and the tpl. Global variables are accessed by the data task pointer and must be between the dtp and the apl. Recall that locals are used by internal procedure calls and globals are used by all procedures in a task.

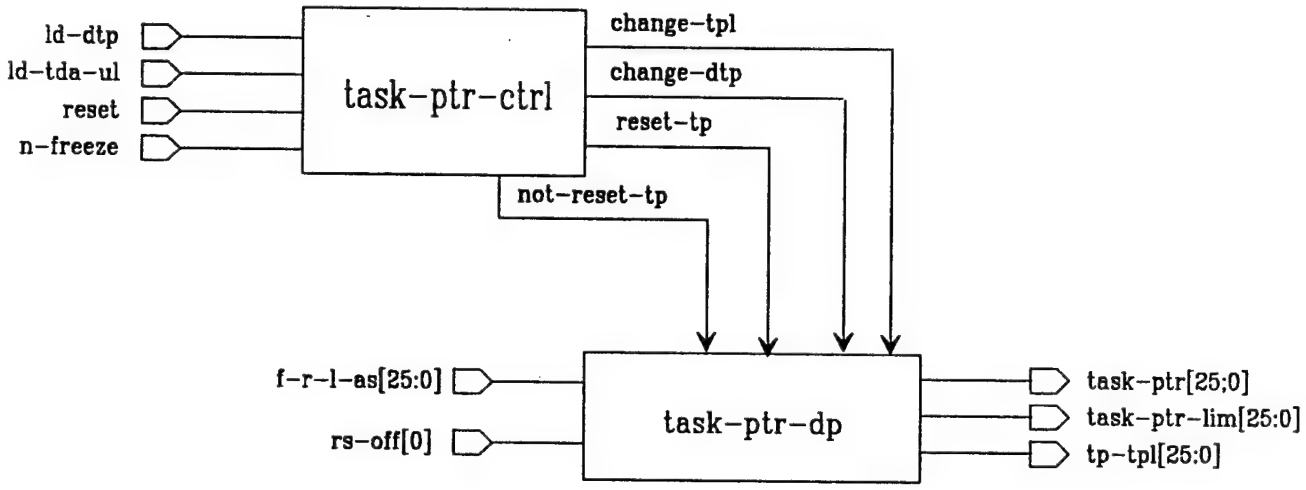
adr<apl -> adr–under
adr<tp -> task–under
adr>=tpl -> adr–over
adr>=apl -> task–over



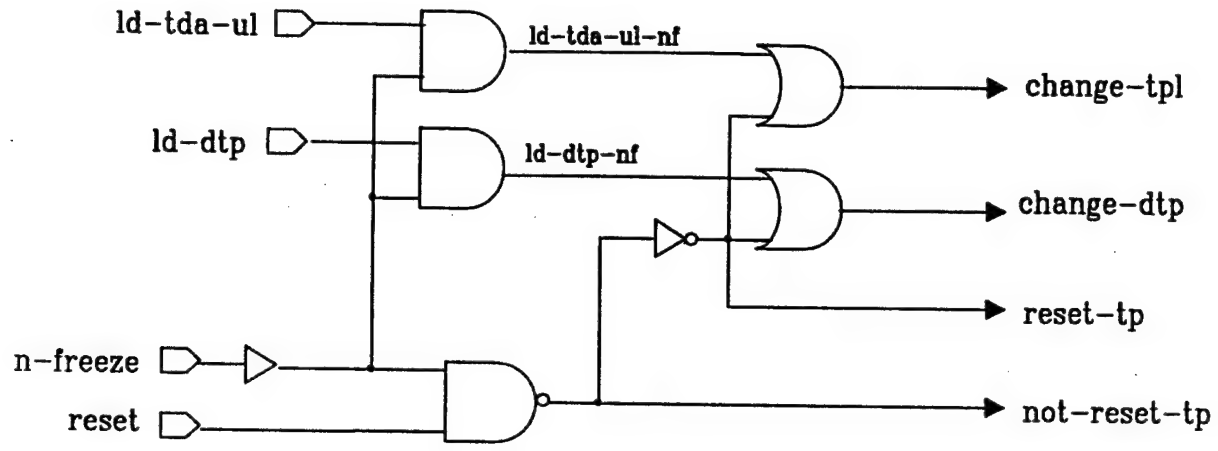
IF: (reset) OR (clr–err–flag) OR (flush AND ERROR LAST CYCLE AND NO ERROR 2 CYCLES AGO)
THEN RESET THE FLAG

(NOTE: flush zeros out errors on current cycle in over–under–mod/ctrl)

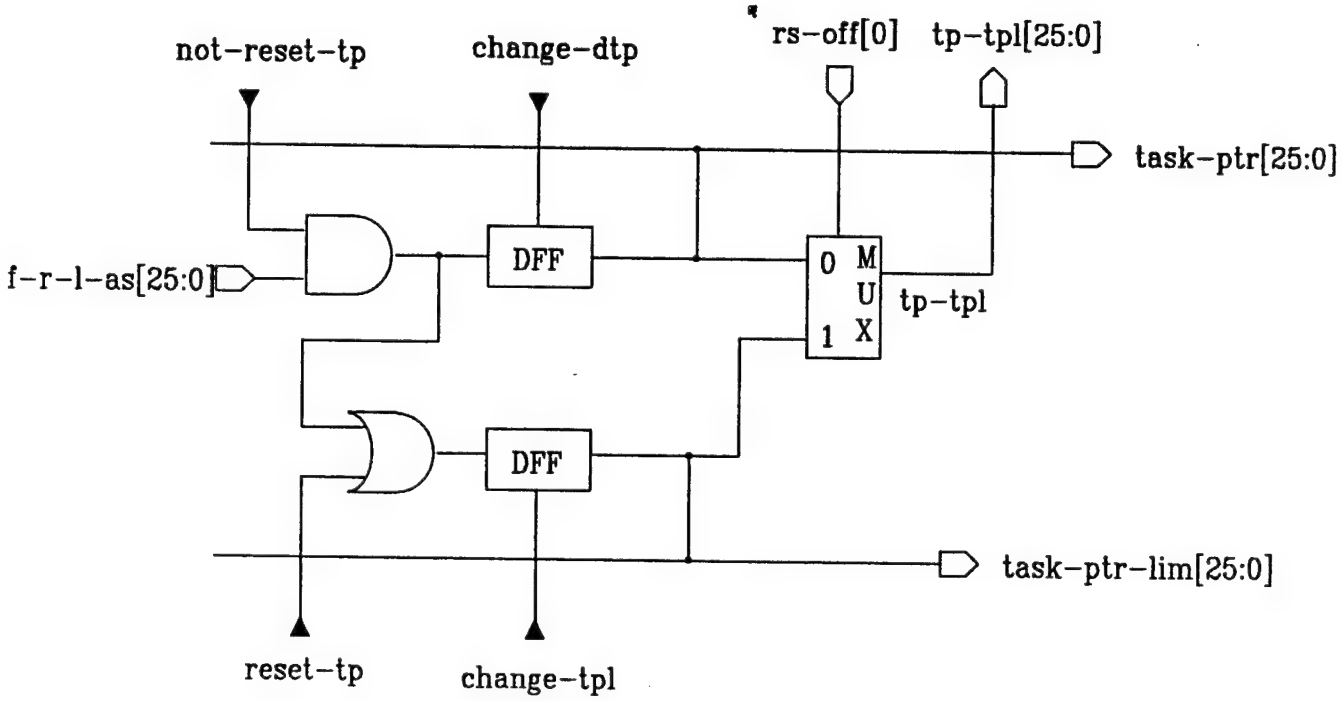
super–ctrl/over–under–mod/flags


ld–dtp
ld–tda–ul
reset
n–freeze
task–ptr–ctrl
change–tpl
change–dtp
reset–tp
not–reset–tp
f–r–l–as[25:0]
rs–off[0]
task–ptr–dp
task–ptr[25;0]
task–ptr–lim[25:0]
tp–tpl[25:0]

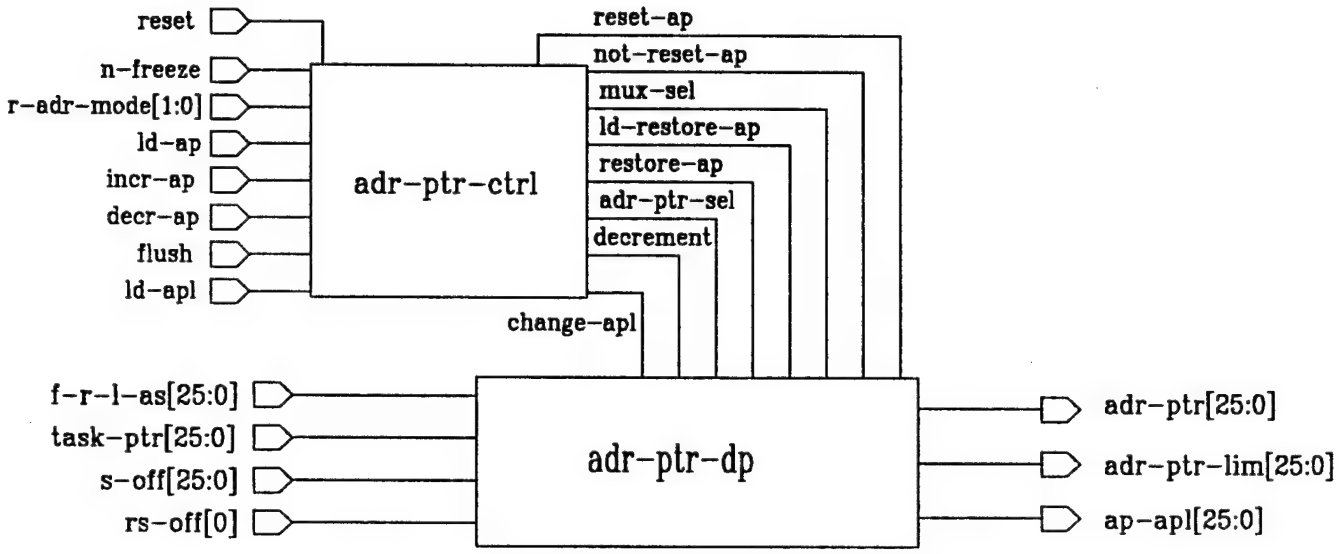
task–ptr–mod



task–ptr–ctrl

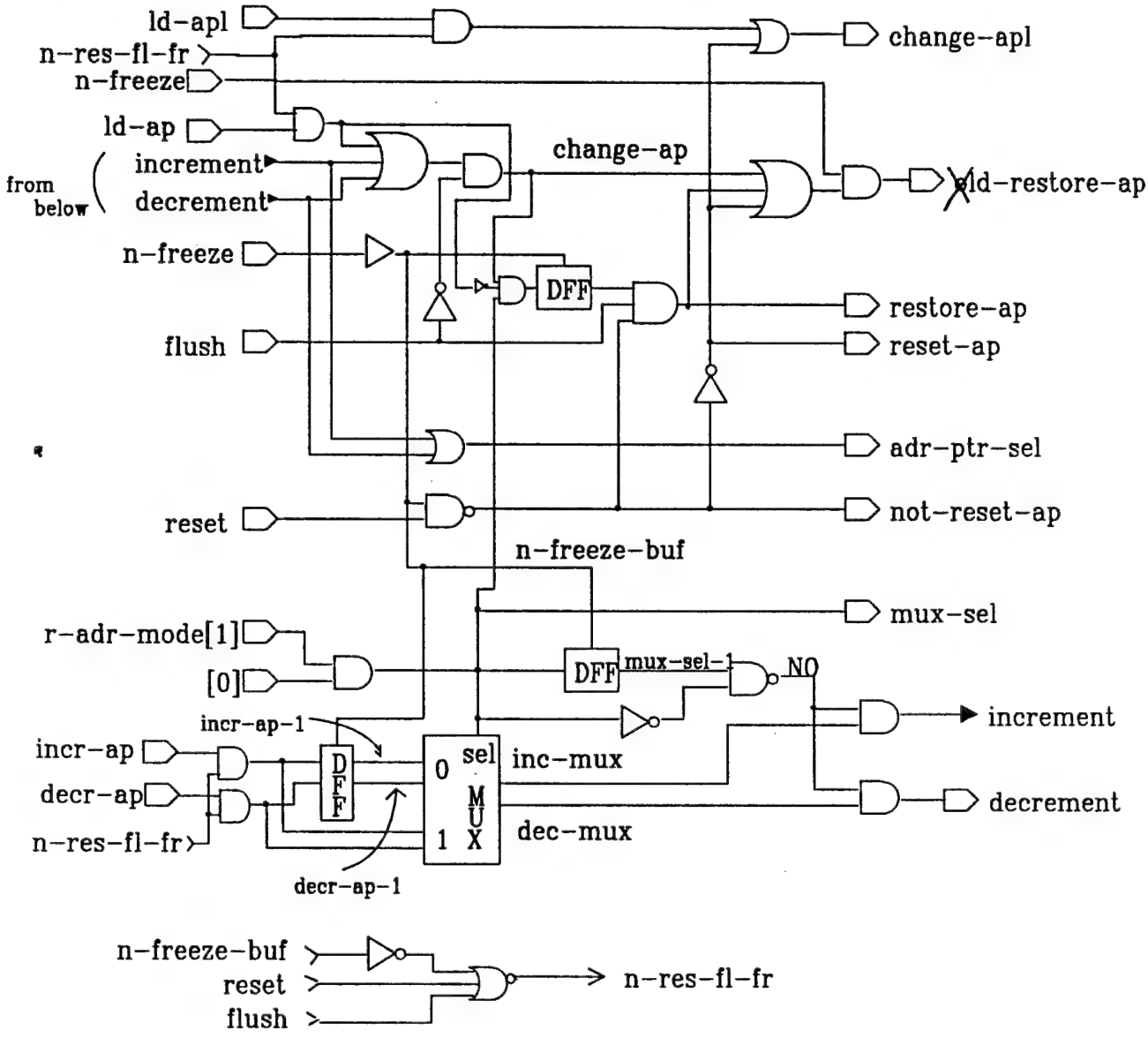


task–ptr–dp


reset
n-freeze
r-adr-mode[1:0]
ld-ap
incr-ap
decr-ap
flush
ld-apl
adr-ptr-ctrl
reset-ap
not-reset-ap
mux-sel
ld-restore-ap
restore-ap
adr-ptr-sel
decrement
change-apl
f-r-l-as[25:0]
task-ptr[25:0]
s-off[25:0]
rs-off[0]
adr-ptr-dp
adr-ptr[25:0]
adr-ptr-lim[25:0]
ap-apl[25:0]

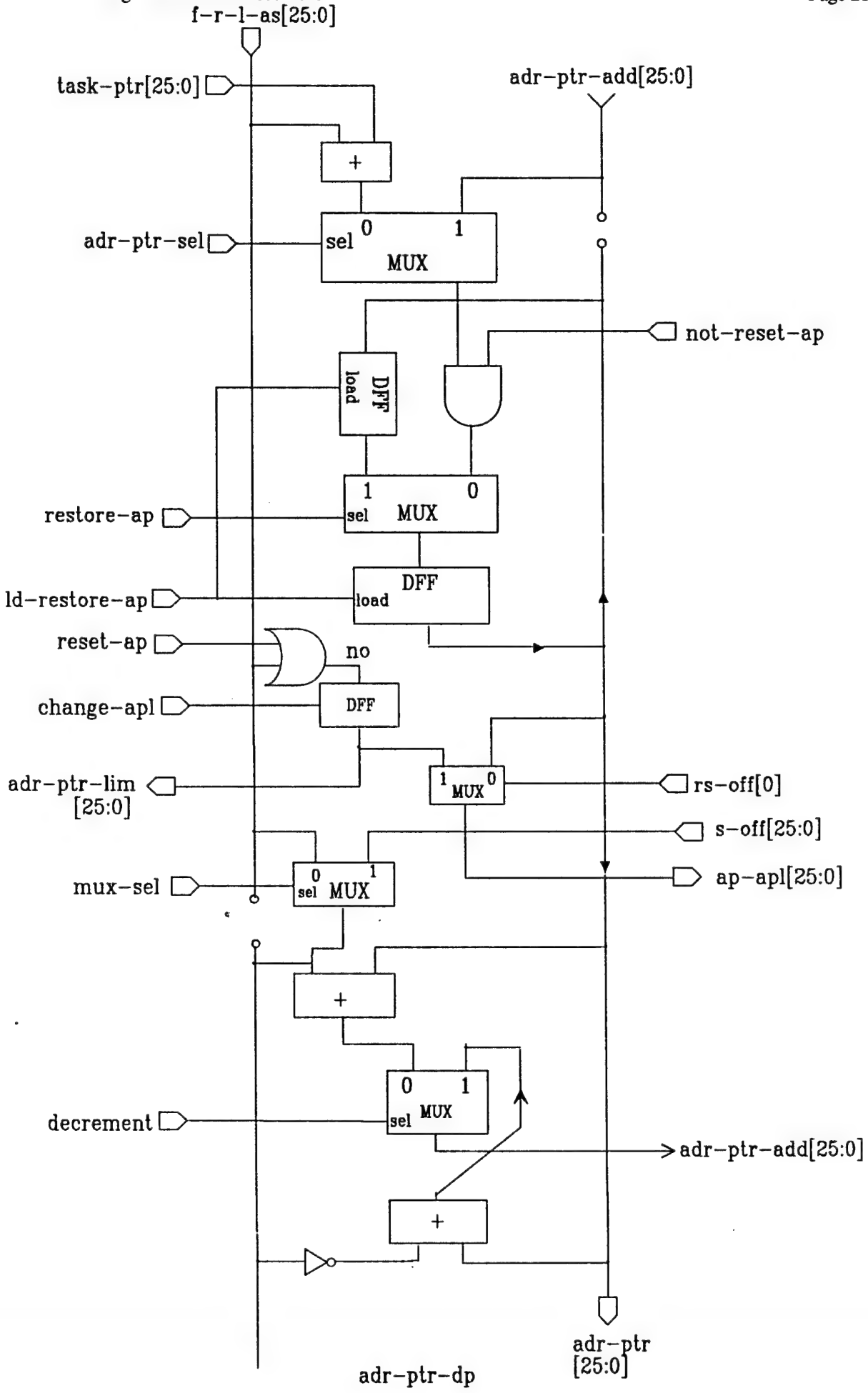
adr-ptr-mod

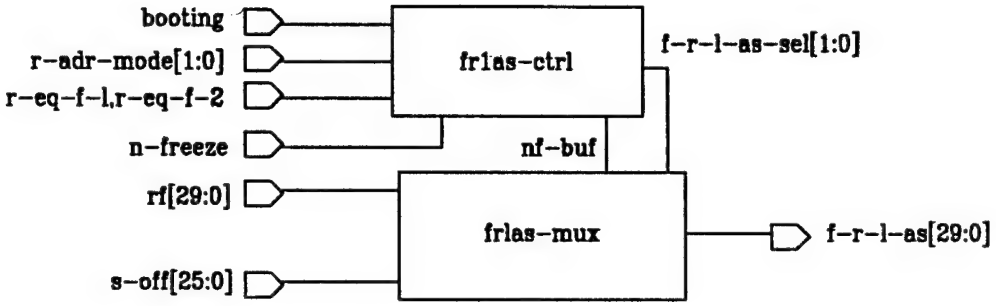
Condition	Source	adr–ptr –sel	change –ap	if	use
ld–ap	f–r–1–as+tp	0	1	r–adr–mode[1:0]=11	incr–ap/decr–ap
(z^{-1})(incr–ap,decr–ap) r–adr–mode≠11	ap+f–r–1–as	1	1	r–adr–mode[1:0]≠11	s–off (z^{-1})(incr–ap/decr–ap) f–r–1–as
incr–ap,decr–ap r–adr–mode=11	ap+s–off	1	1	(z^{-1})(r–adr–mode=11) AND (r–adr–mode≠11)	don't increment *(see below)



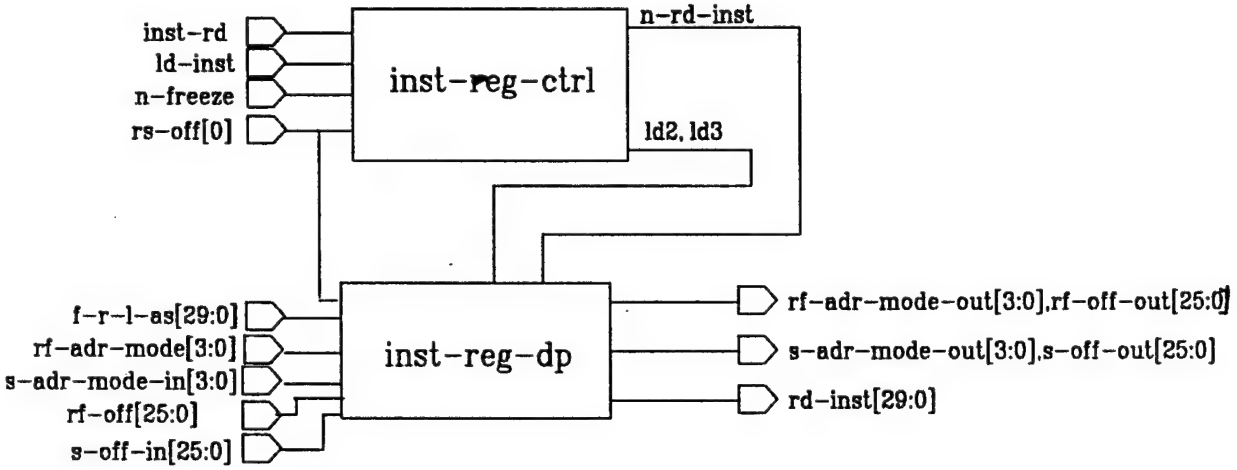
*	Time	r–adr–mode	(z^{-1})r–adr–mode	incr–ap	incr–mux	incr–ap–1
	1	11	00	1	1	0
	2	00	11	0	1	1

adr–ptr–ctrl


f-r-l-as[25:0]
task-ptr[25:0]
adr-ptr-add[25:0]
+
adr-ptr-sel
sel 0 1
MUX
not-reset-ap
load DFF
1 0
restore-ap
sel MUX
DFF
ld-restore-ap
load
reset-ap
no
change-apl
DFF
adr-ptr-lim
[25:0]
1 MUX 0
rs-off[0]
s-off[25:0]
mux-sel
0 1
sel MUX
ap-apl[25:0]
+
0 1
decrement
sel MUX
adr-ptr-add[25:0]
+
adr-ptr
[25:0]
adr-ptr-dp



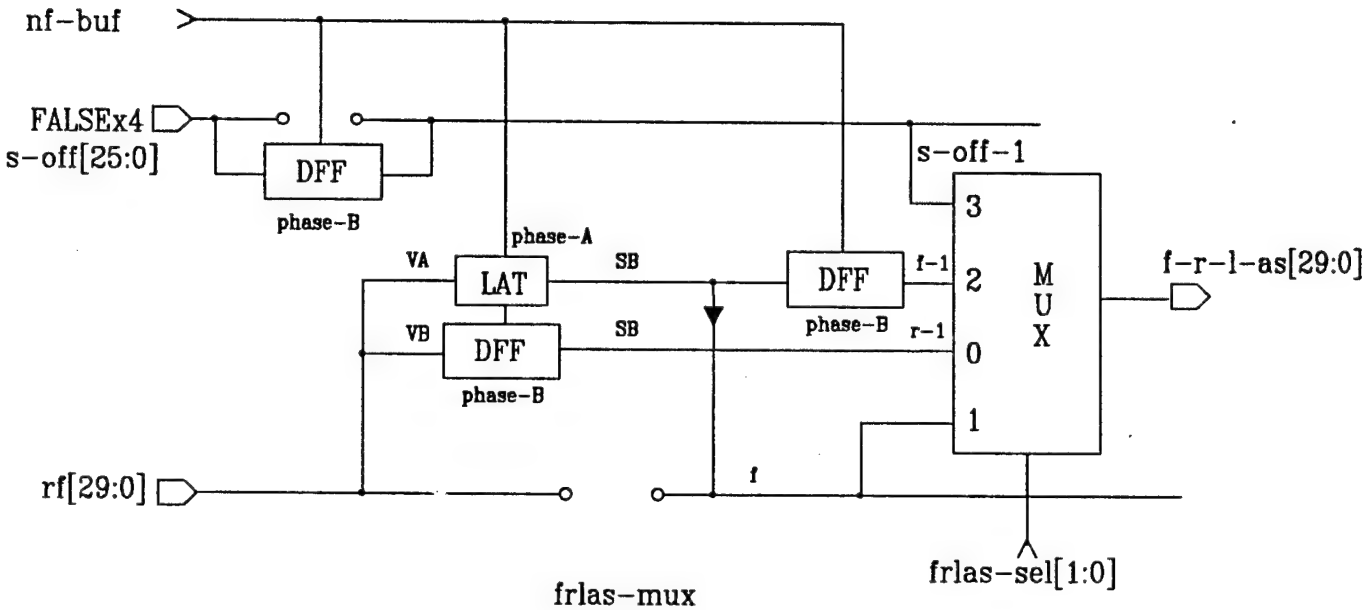
fr1as_–mod



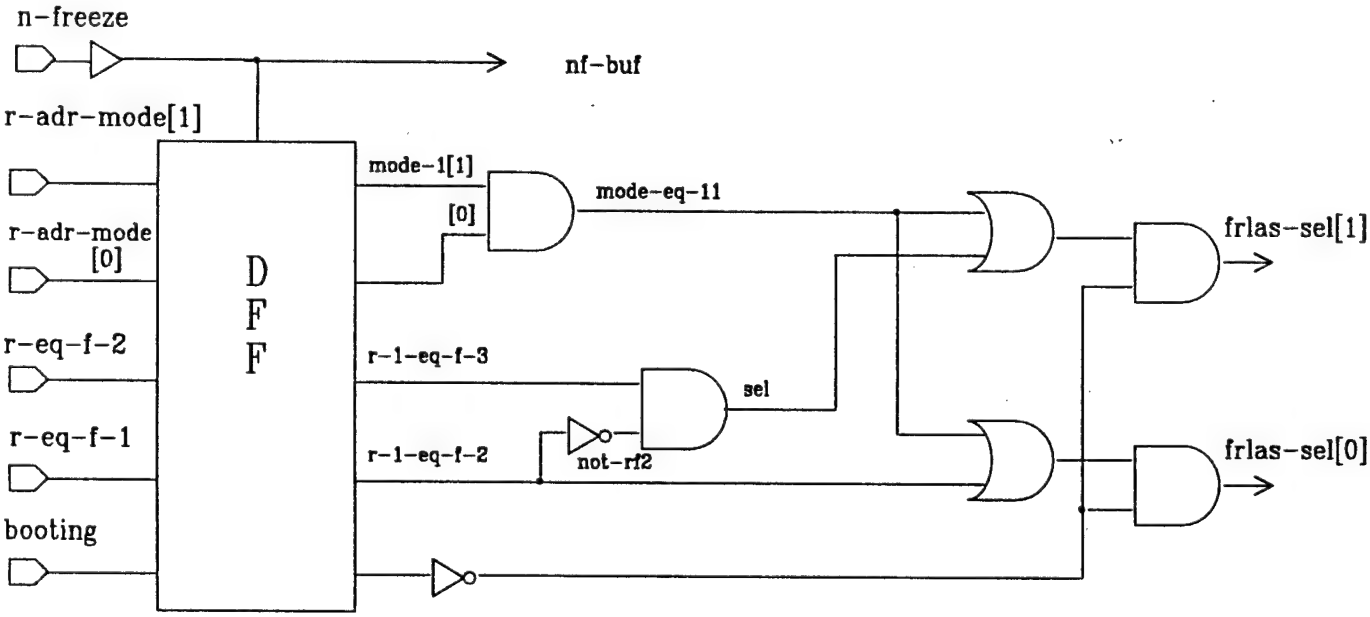
inst–reg–mod

Condition	Source	sel bits
r-adr-mode-1=11	s-off-1	11
(z^{-1}) r-eq-f-1	f	01
(z^{-1})r-eq-f-2&NOT(z^{-1})r-eq-f-1	f-1	10
else	r-1	00

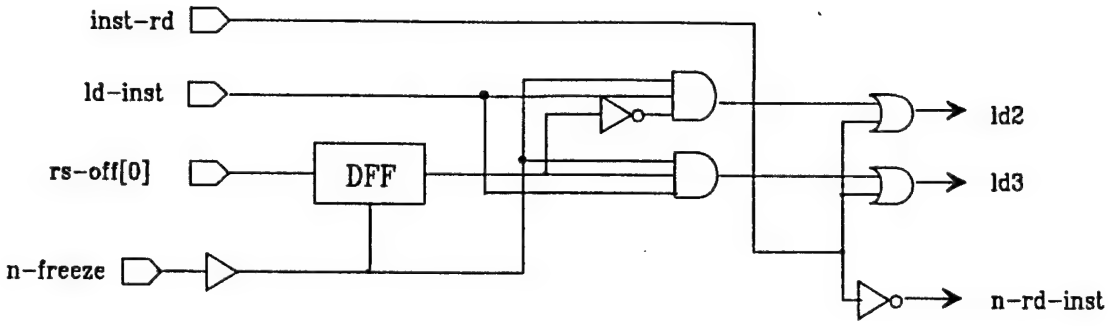
(z^{-1}) r-eq-f-1	(z^{-1}) r-eq-f-2	Source
0	0	r-1
0	1	f-1
1	0	f
1	1	f



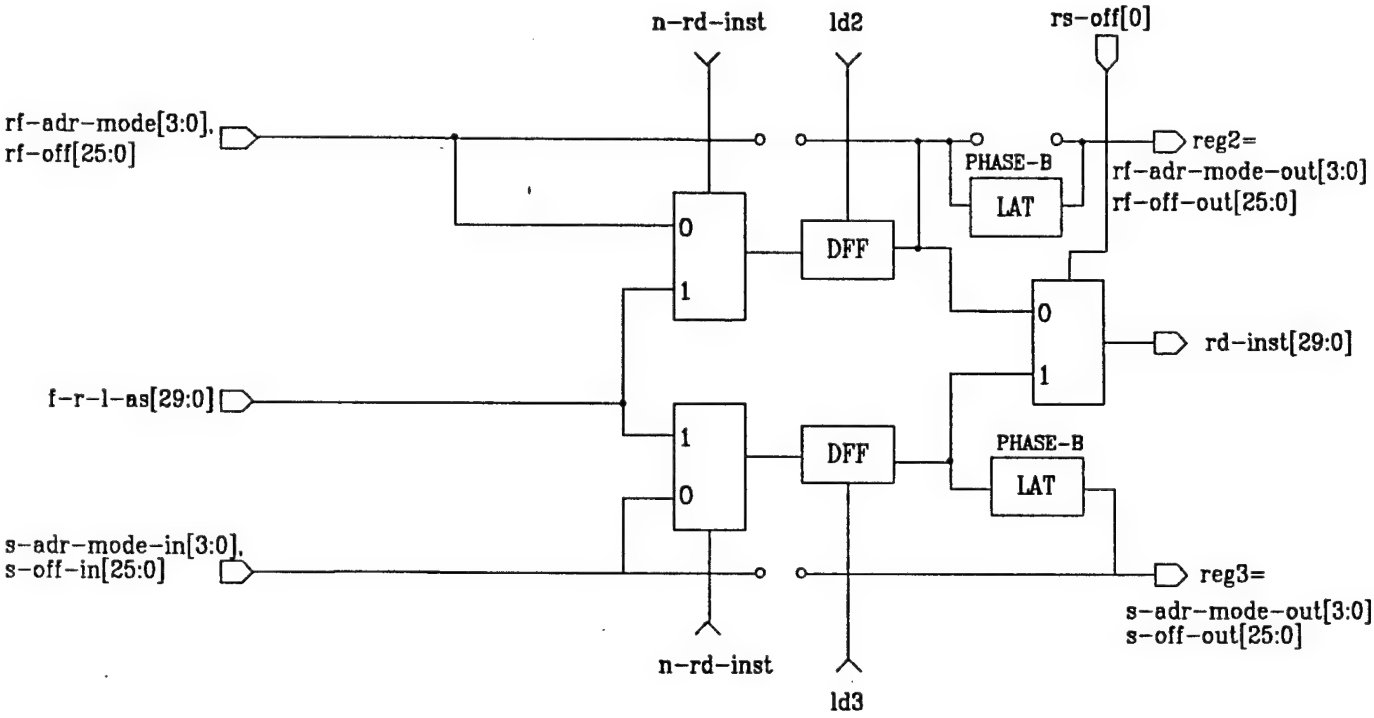
frlas-mux



frlas-ctrl



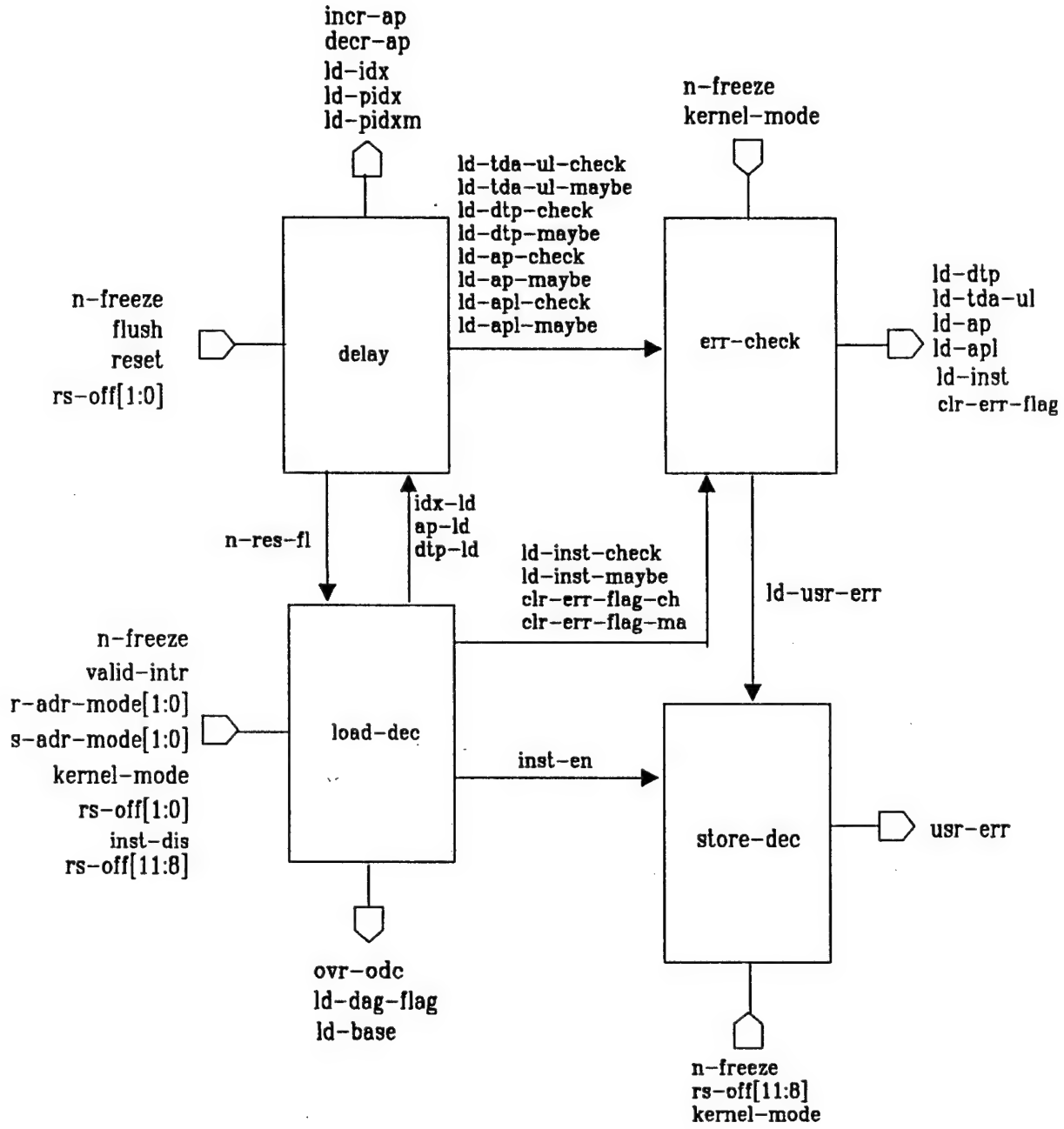
inst–reg–ctrl



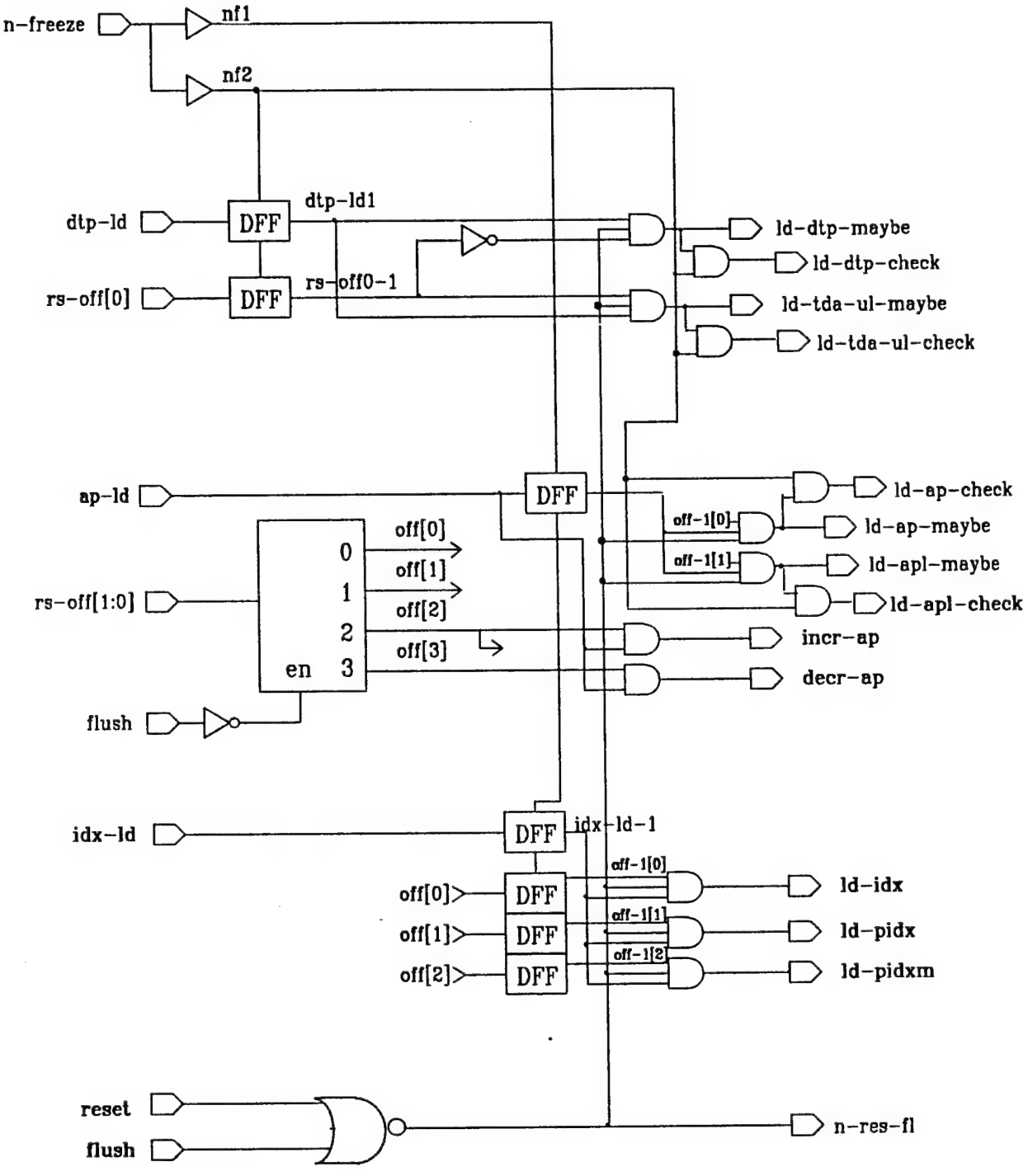
inst–reg–dp

	inst	register
F–adr–mode	89:86	2
R–adr–mode	85:82	2
S–adr–mode	81:78	3
F–off	77:52	2
R–off	51:26	2
S–off	25:0	3

inst–reg–mod

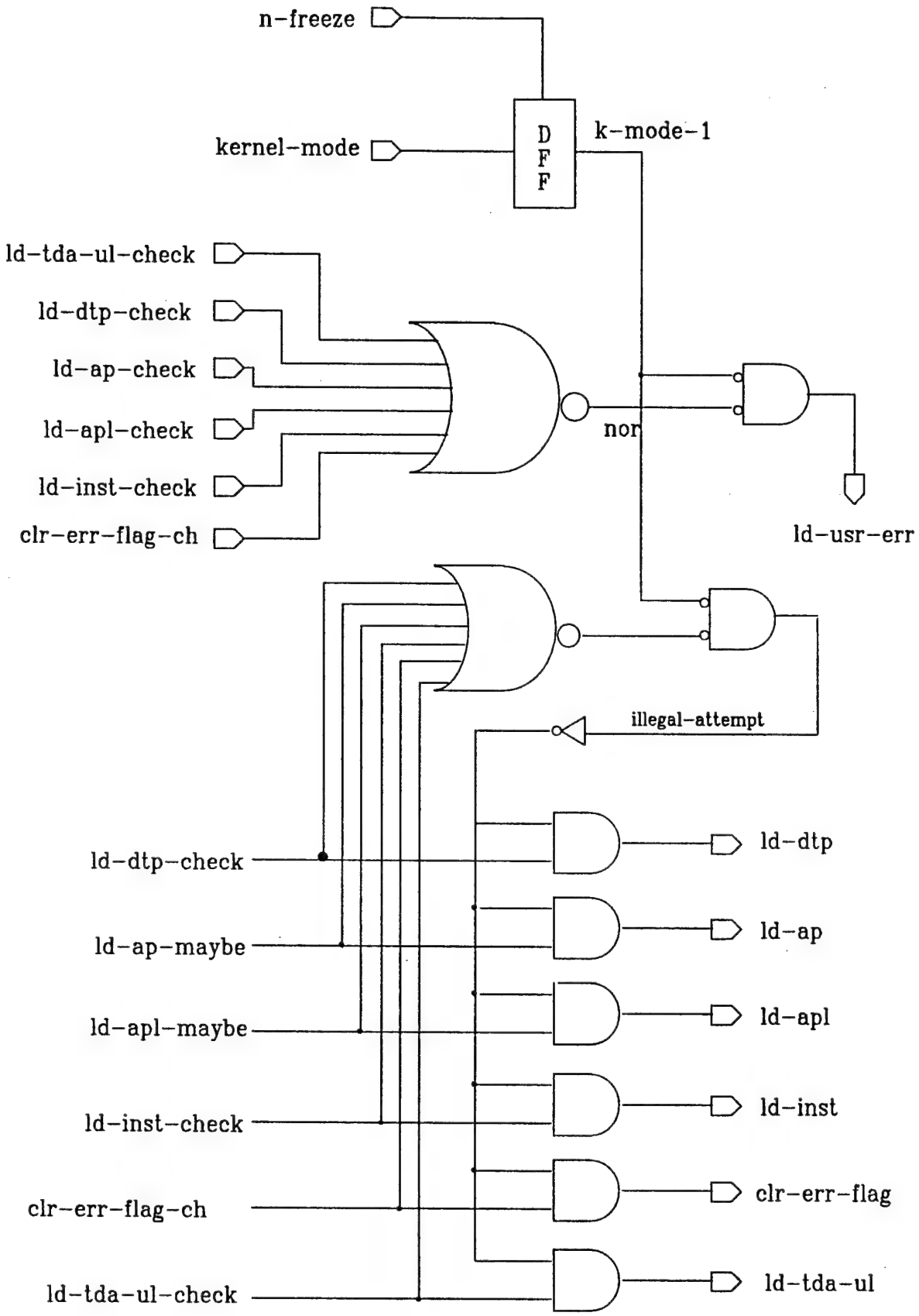

incr–ap
decr–ap
ld–idx
ld–pidx
ld–pidxm
n–freeze
kernel–mode
ld–tda–ul–check
ld–tda–ul–maybe
ld–dtp–check
ld–dtp–maybe
ld–ap–check
ld–ap–maybe
ld–apl–check
ld–apl–maybe
n–freeze
flush
reset
rs–off[1:0]
delay
err–check
ld–dtp
ld–tda–ul
ld–ap
ld–apl
ld–inst
clr–err–flag
idx–ld
ap–ld
dtp–ld
n–res–fl
ld–inst–check
ld–inst–maybe
clr–err–flag–ch
clr–err–flag–ma
ld–usr–err
n–freeze
valid–intr
r–adr–mode[1:0]
s–adr–mode[1:0]
kernel–mode
rs–off[1:0]
inst–dis
rs–off[11:8]
load–dec
inst–en
store–dec
usr–err
ovr–odc
ld–dag–flag
ld–base
n–freeze
rs–off[11:8]
kernel–mode

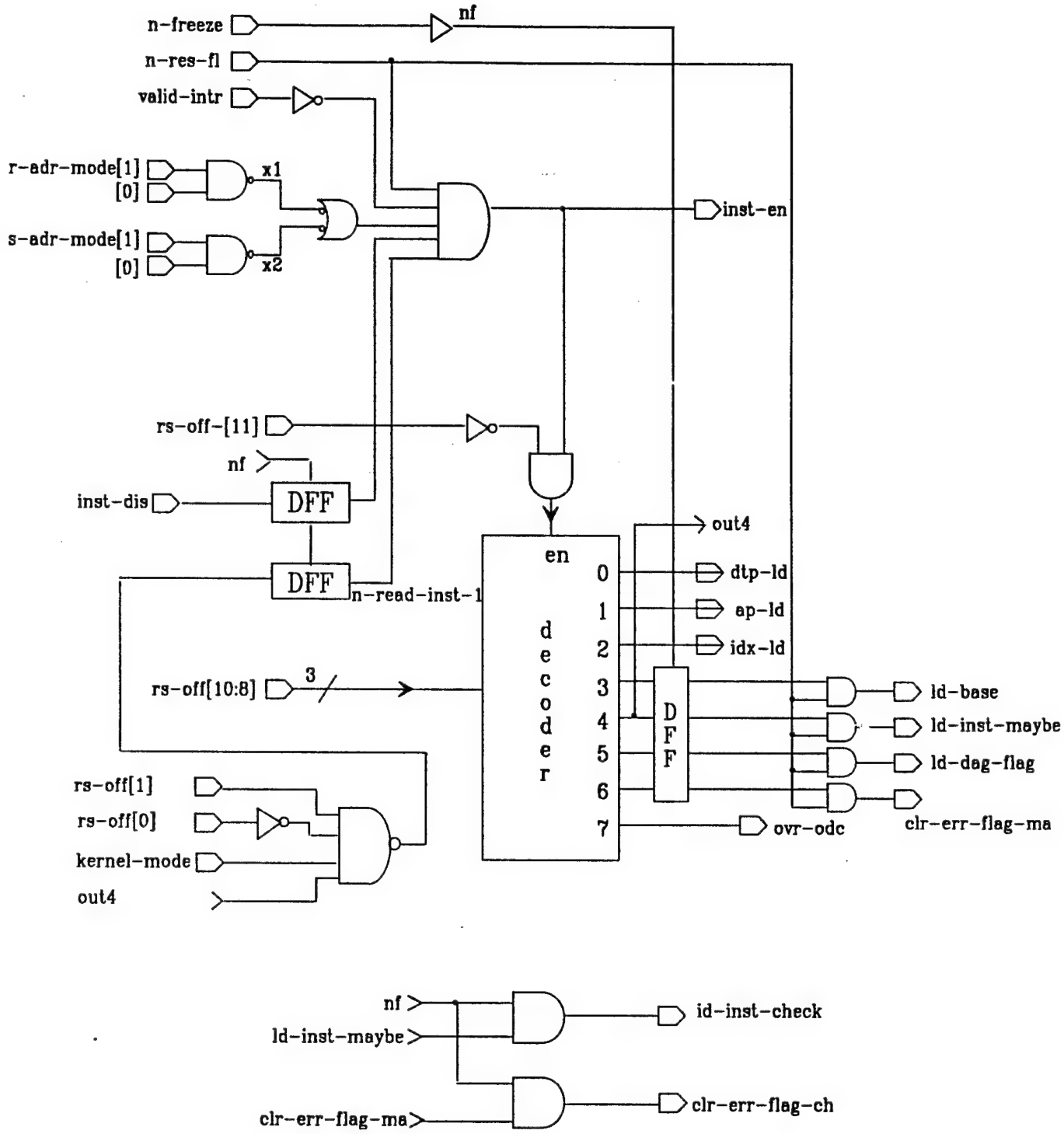
decoders



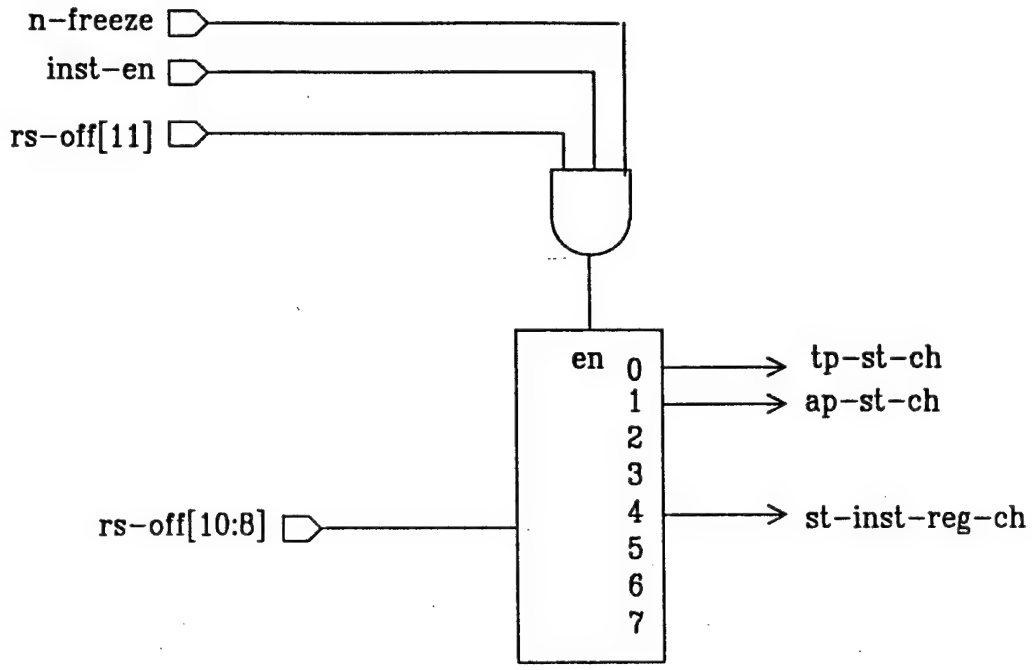
delay

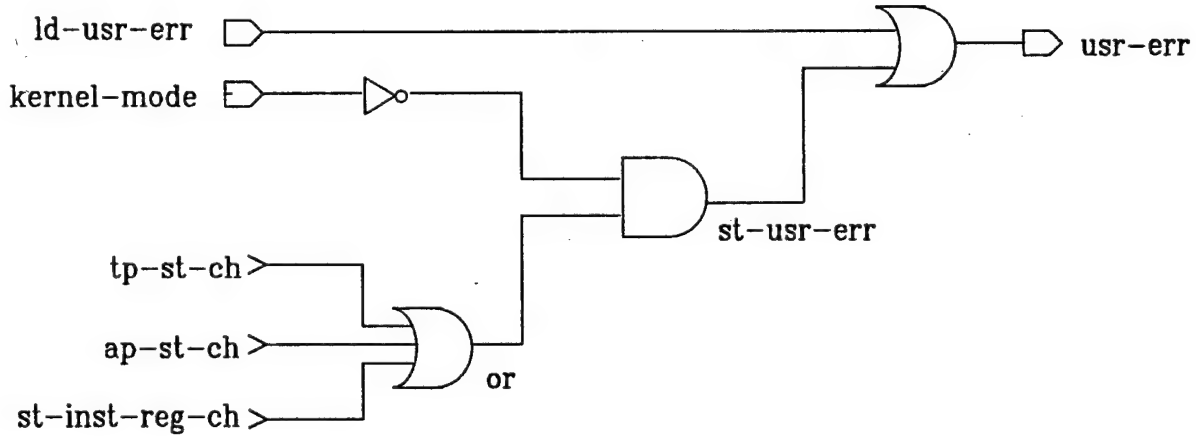
decoders


n–freeze
kernel–mode
D
F
F
k–mode–1
ld–tda–ul–check
ld–dtp–check
ld–ap–check
ld–apl–check
ld–inst–check
clr–err–flag–ch
nor
ld–usr–err
illegal–attempt
ld–dtp–check
ld–ap–maybe
ld–apl–maybe
ld–inst–check
clr–err–flag–ch
ld–tda–ul–check
ld–dtp
ld–ap
ld–apl
ld–inst
clr–err–flag
ld–tda–ul
err–check
decoders

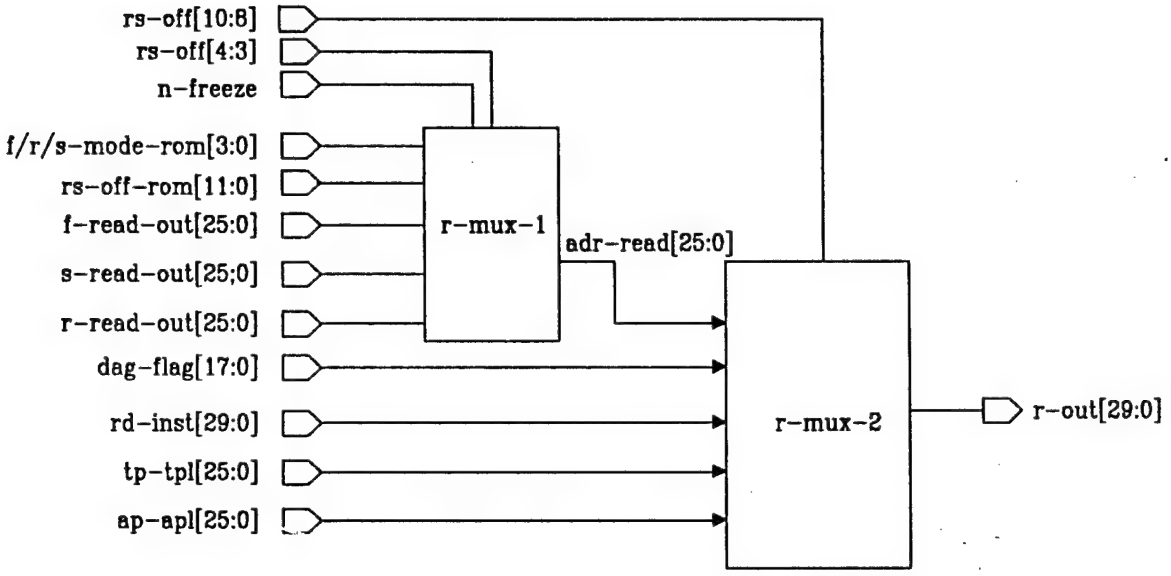

n-freeze
nf
n-res-fl
valid-intr
r-adr-mode[1]
[0]
x1
s-adr-mode[1]
[0]
x2
inst-en
rs-off-[11]
nf
inst-dis
DFF
DFF
n-read-inst-1
out4
en
decoder
0
1
2
3
4
5
6
7
dtp-ld
ap-ld
idx-ld
DFF
rs-off[10:8]
3
ld-base
ld-inst-maybe
ld-dag-flag
clr-err-flag-ma
ovr-odc
rs-off[1]
rs-off[0]
kernel-mode
out4
nf
ld-inst-maybe
id-inst-check
clr-err-flag-ma
clr-err-flag-ch

load-dec

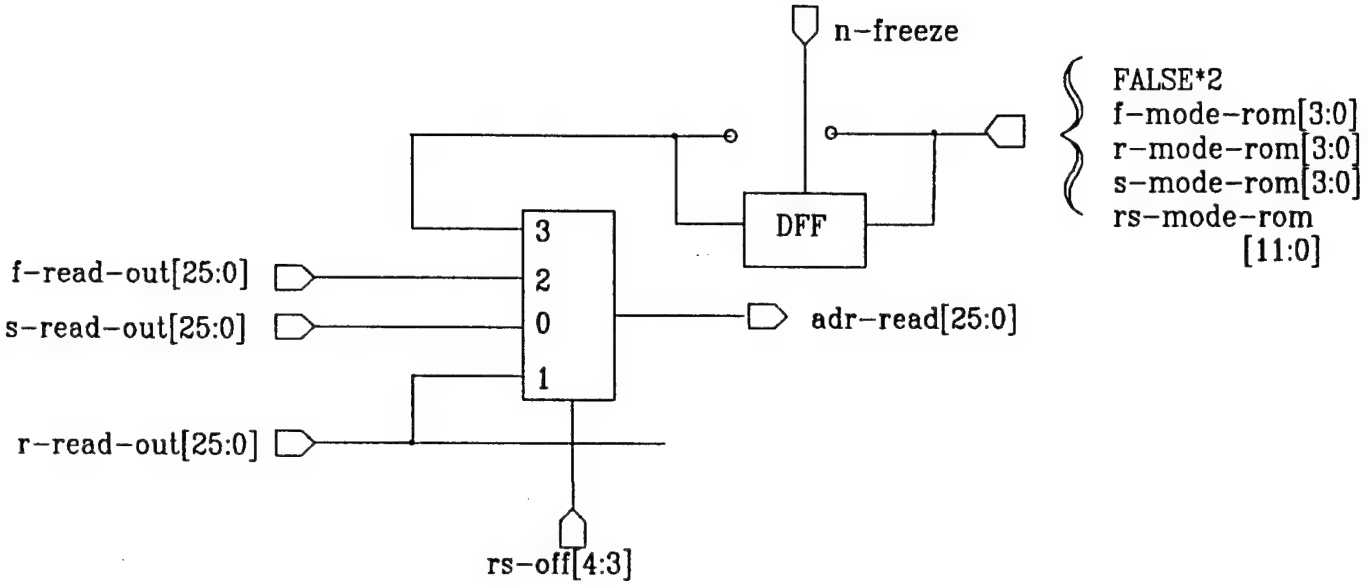




decoders/store-dec

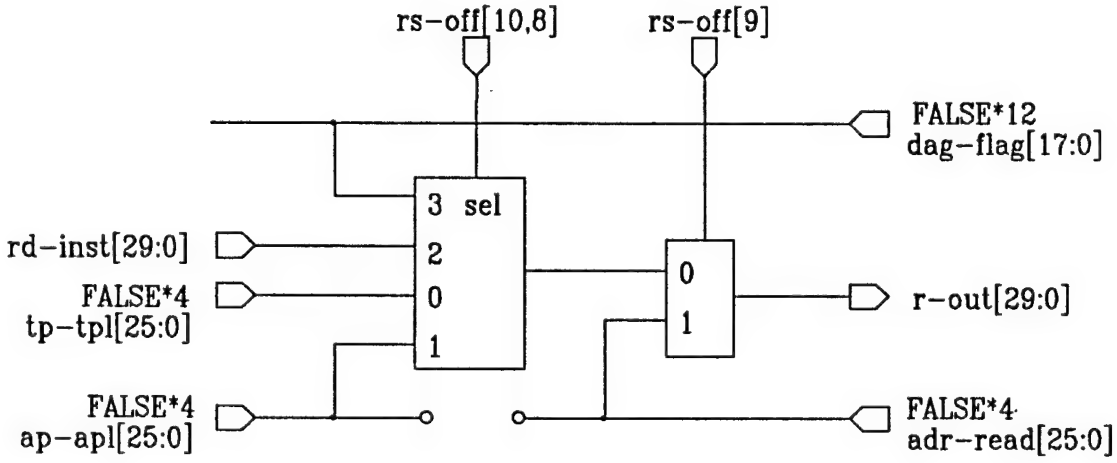

rs–off[10:8]
rs–off[4:3]
n–freeze
f/r/s–mode–rom[3:0]
rs–off–rom[11:0]
f–read–out[25:0]
s–read–out[25;0]
r–read–out[25:0]
dag–flag[17:0]
rd–inst[29:0]
tp–tpl[25:0]
ap–apl[25:0]
r–mux–1
adr–read[25:0]
r–mux–2
r–out[29:0]

r–out–mod



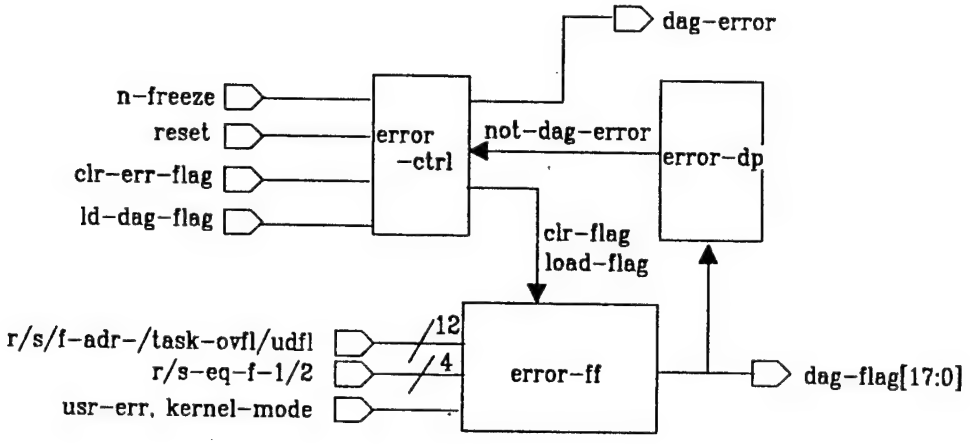
r-mux-1

	rs-off[11:8]		rs-off[10,8]	rs-off[9]
tp-tpl	8	1000	0 0	0
ap-apl	9	1001	0 1	0
adr-read	a,b	1010		1
		1011		1
rd-inst	c	1100	1 0	0
dag-flag	d	1101	1 1	0

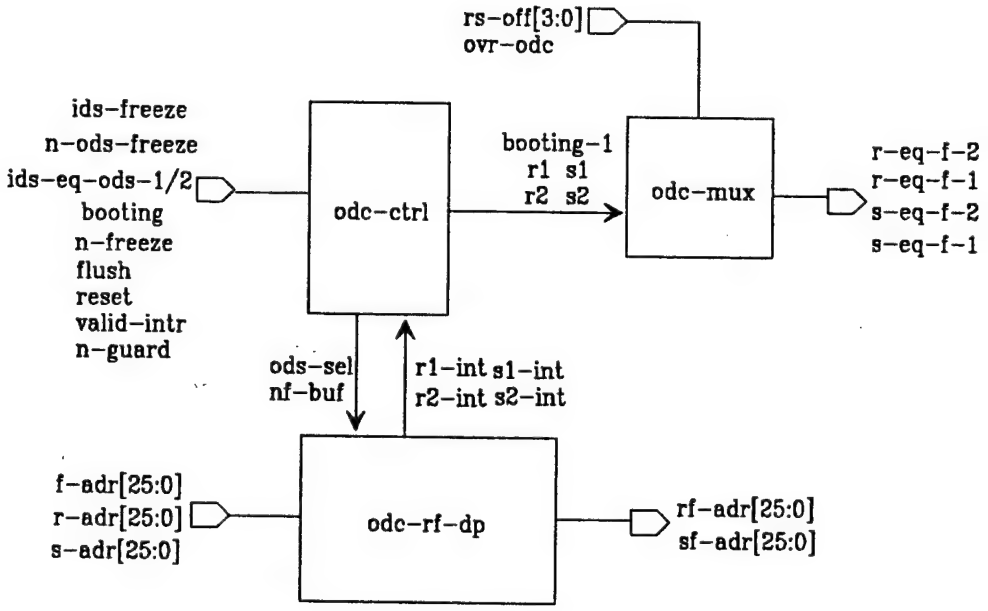


r-mux-2

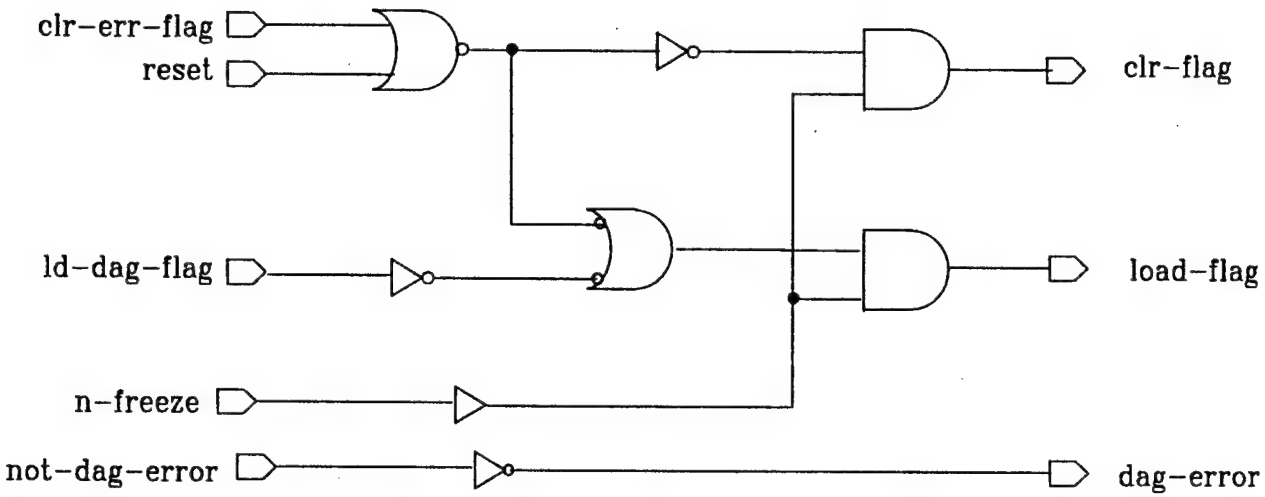
r-out-mod



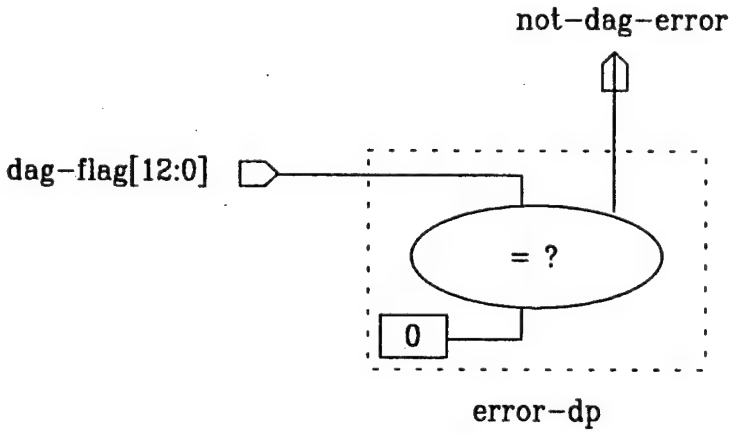
error–mod



odc–rf–mod

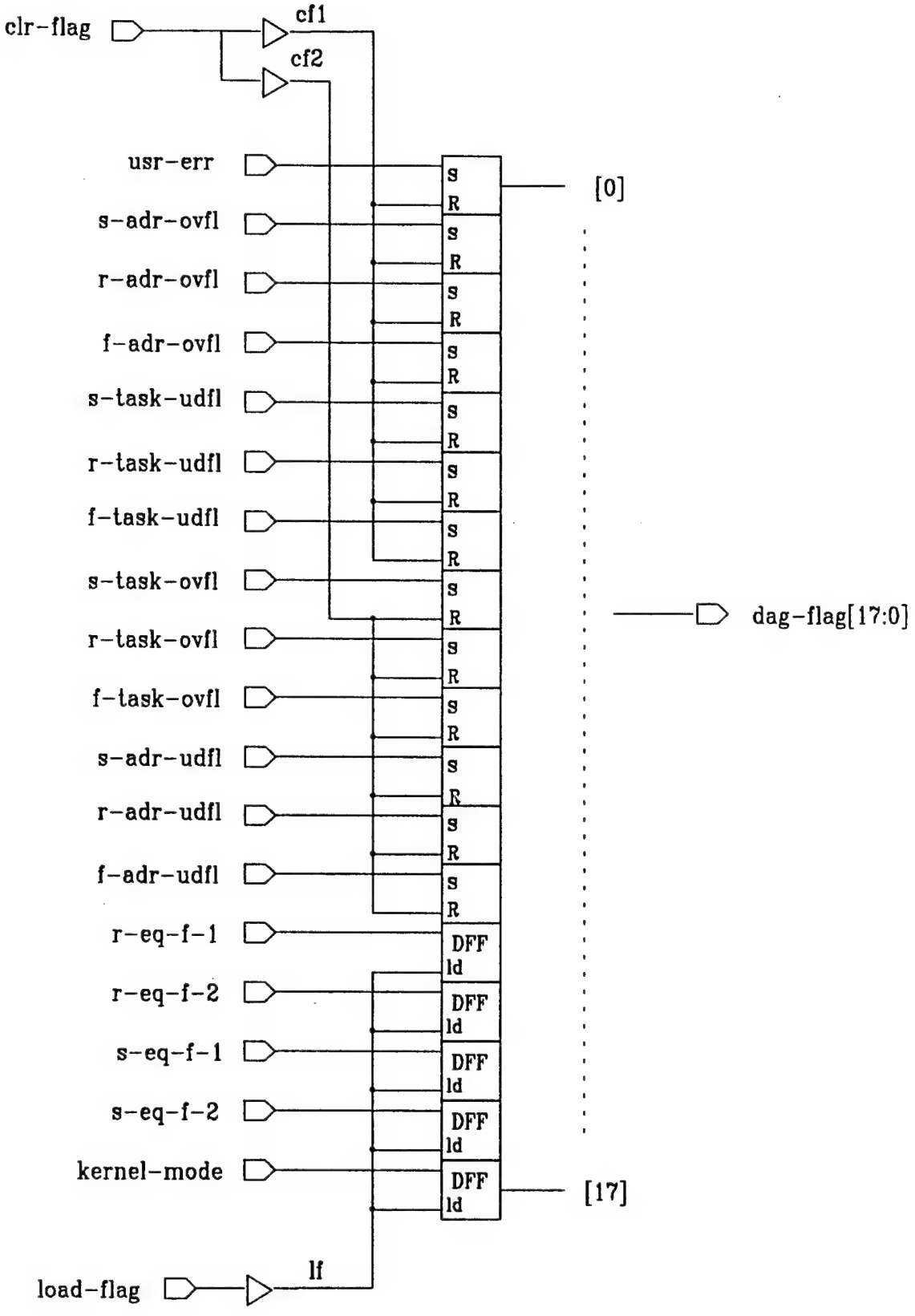


error–ctrl

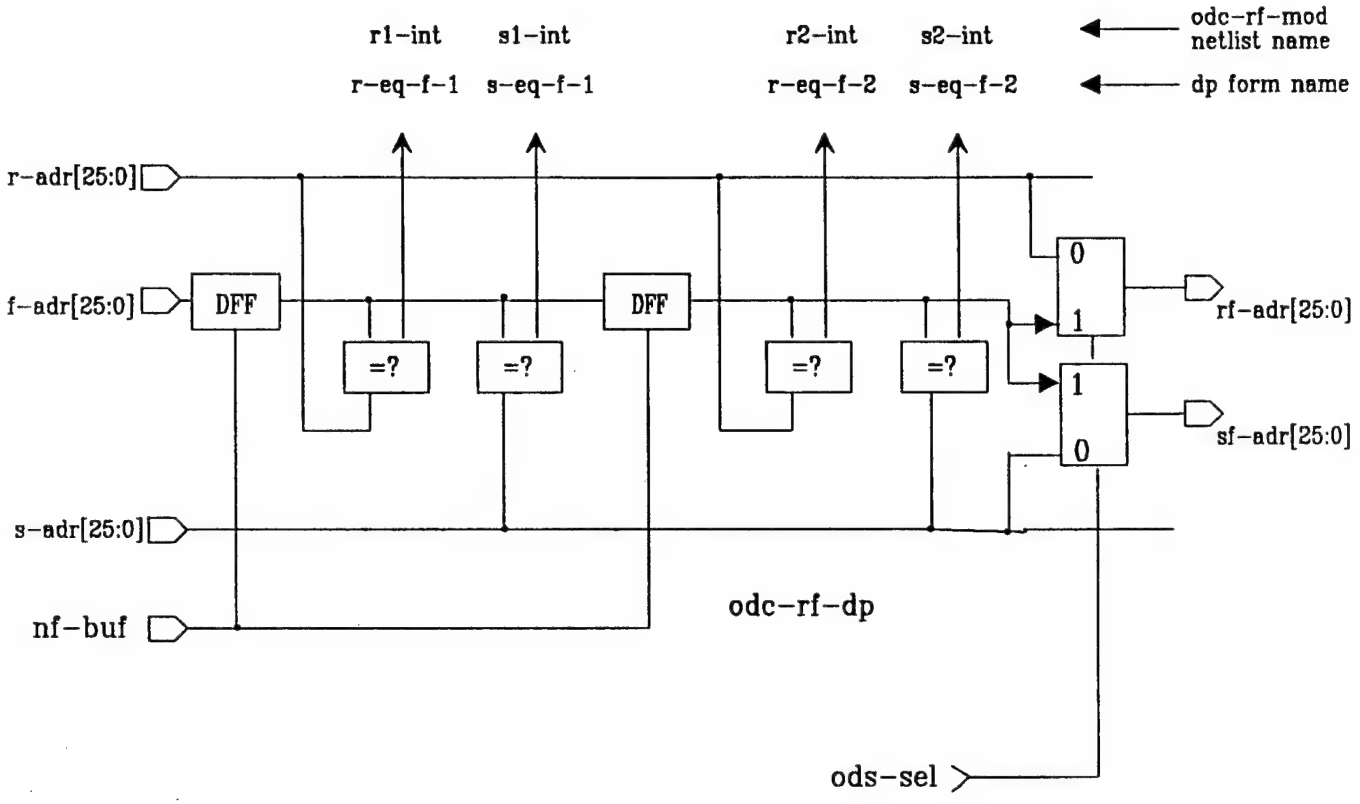


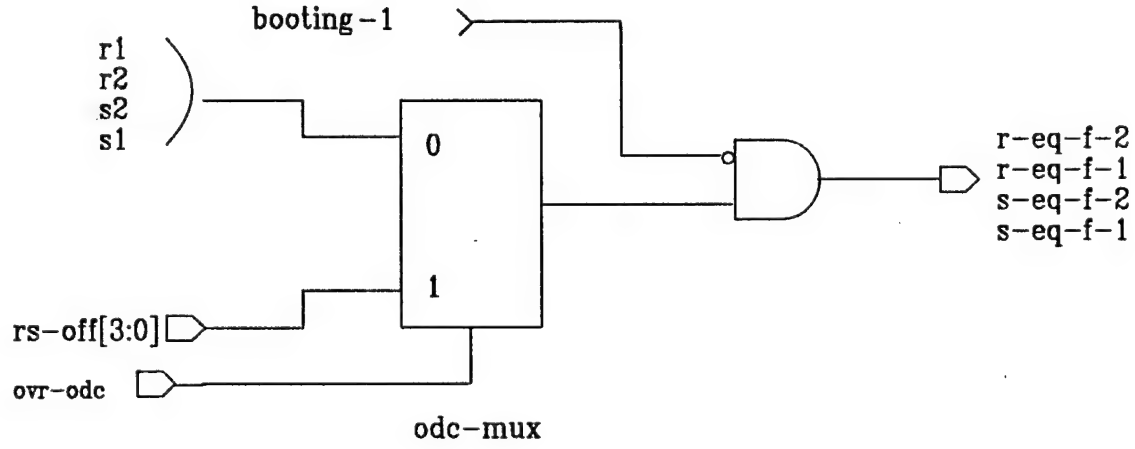
error–dp

error–mod

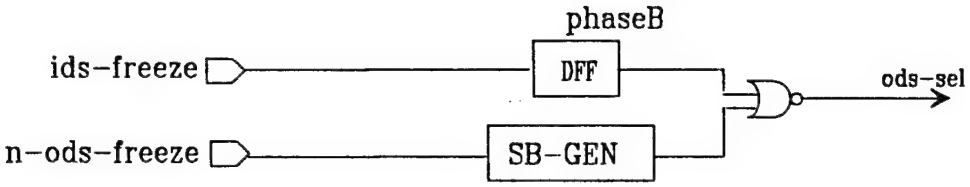

clr-flag
cf1
cf2
usr-err
s-adr-ovfl
r-adr-ovfl
f-adr-ovfl
s-task-udfl
r-task-udfl
f-task-udfl
s-task-ovfl
r-task-ovfl
f-task-ovfl
s-adr-udfl
r-adr-udfl
f-adr-udfl
r-eq-f-1
r-eq-f-2
s-eq-f-1
s-eq-f-2
kernel-mode
load-flag
lf
S
R
DFF
ld
[0]
[17]
dag-flag[17:0]

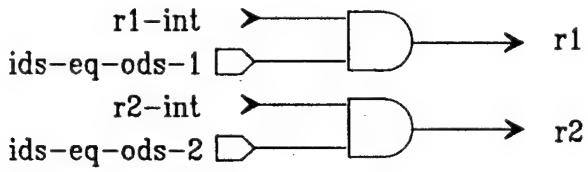
error-ff

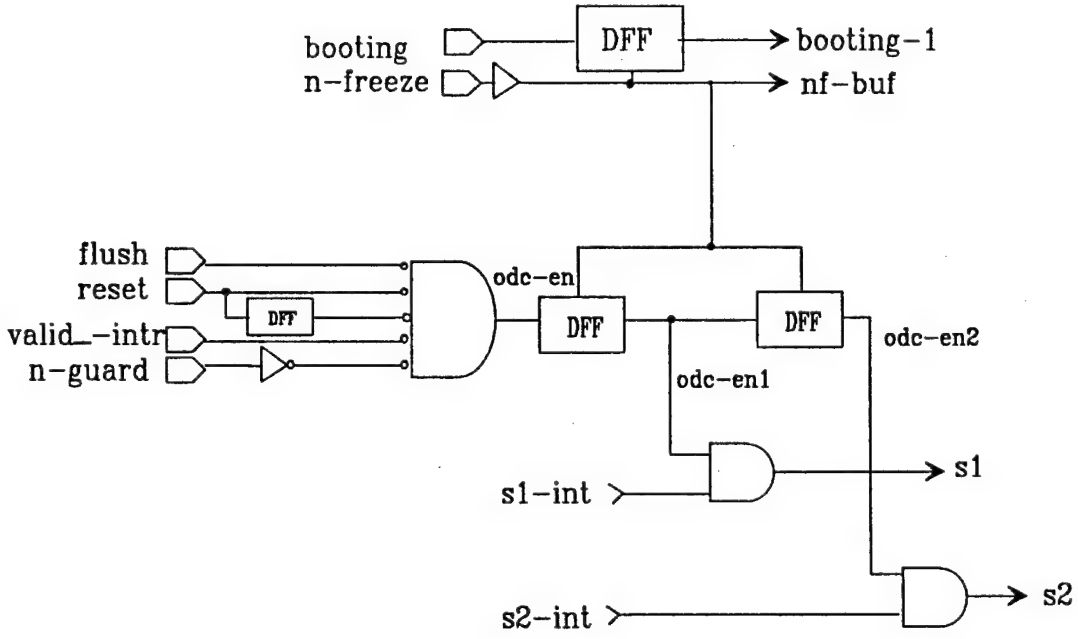

r1-int
s1-int
r2-int
s2-int
odc-rf-mod
netlist name
r-eq-f-1
s-eq-f-1
r-eq-f-2
s-eq-f-2
dp form name
r-adr[25:0]
f-adr[25:0]
DFF
DFF
=?
=?
=?
=?
0
1
1
0
rf-adr[25:0]
sf-adr[25:0]
s-adr[25:0]
nf-buf
odc-rf-dp
ods-sel


booting-1
r1
r2
s2
s1
0
1
r-eq-f-2
r-eq-f-1
s-eq-f-2
s-eq-f-1
rs-off[3:0]
ovr-odc
odc-mux

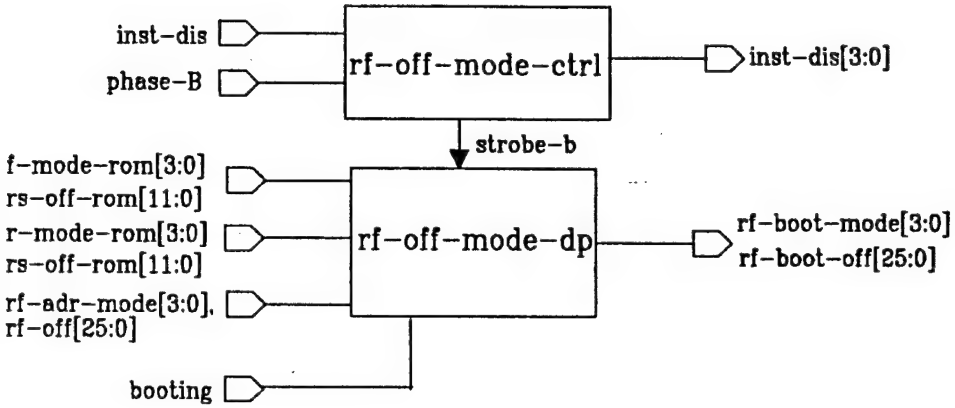
odc-rf-mod


phaseB
ids-freeze
DFF
ods-sel
n-ods-freeze
SB-GEN

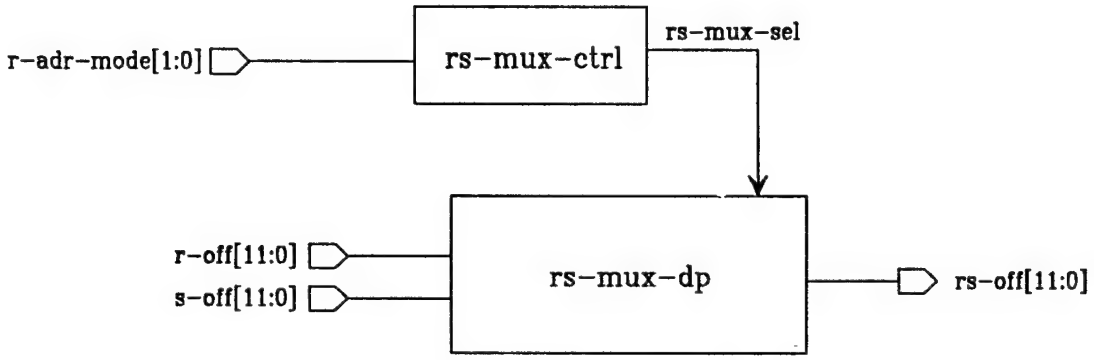

r1-int
ids-eq-ods-1
r1
r2-int
ids-eq-ods-2
r2


booting
n-freeze
DFF
booting-1
nf-buf
flush
reset
valid_-intr
n-guard
DFF
odc-en
DFF
DFF
odc-en2
odc-en1
s1-int
s1
s2-int
s2

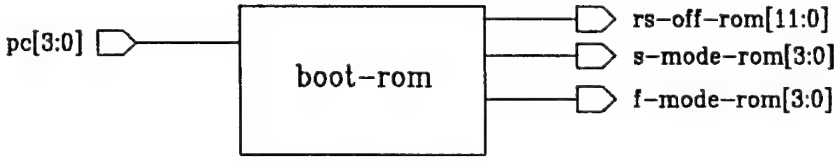
odc-ctrl



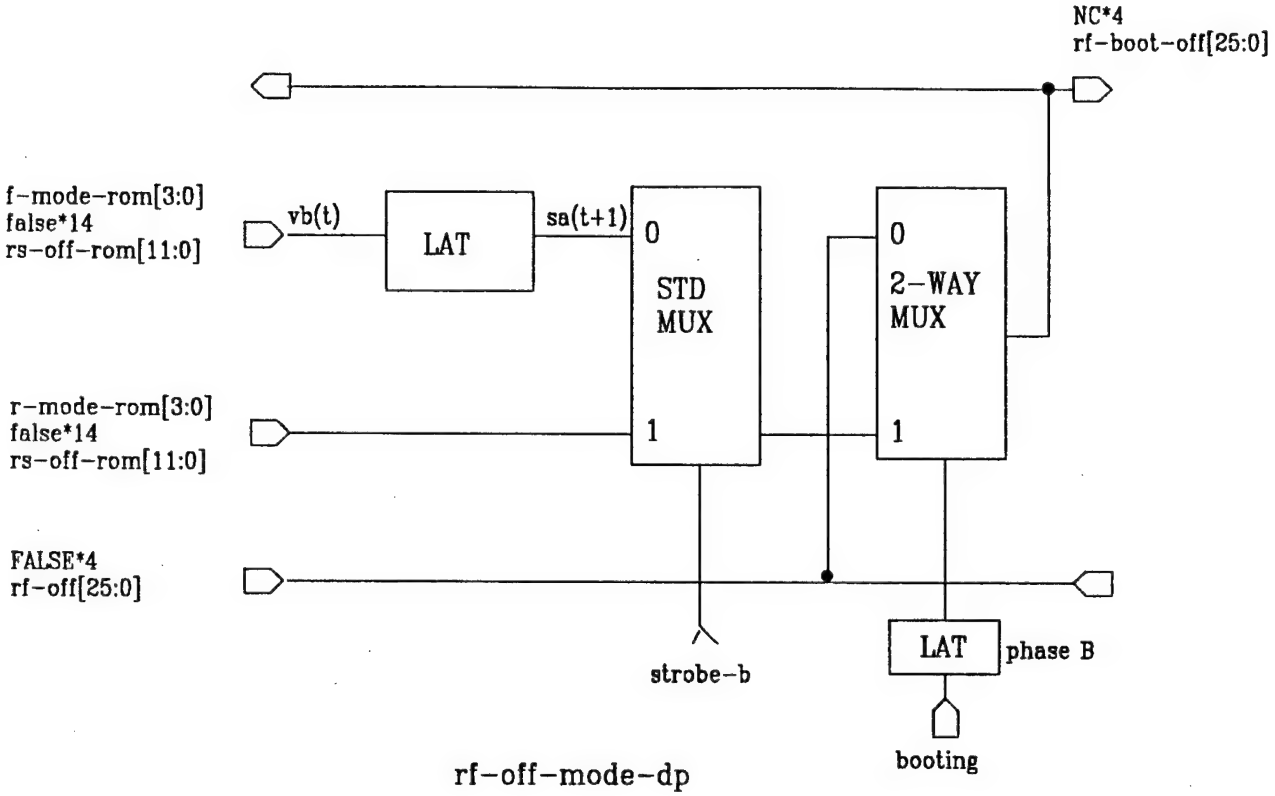
rf–off–mode–mod



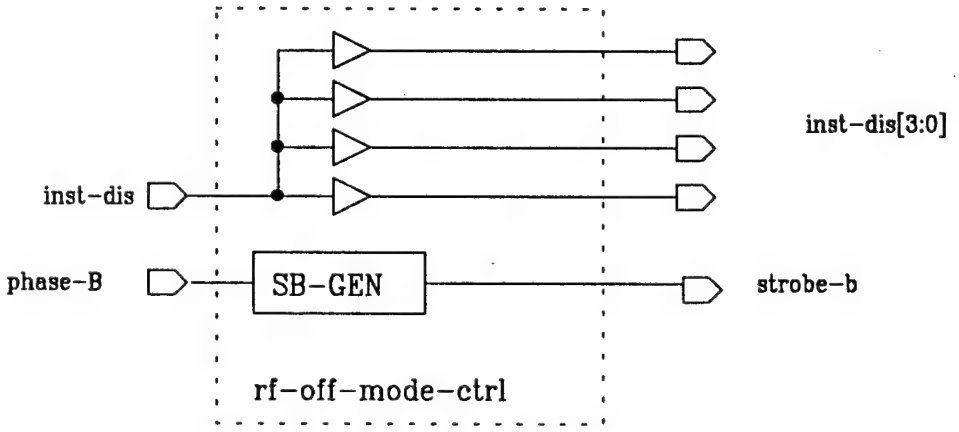
rs–mux–mod



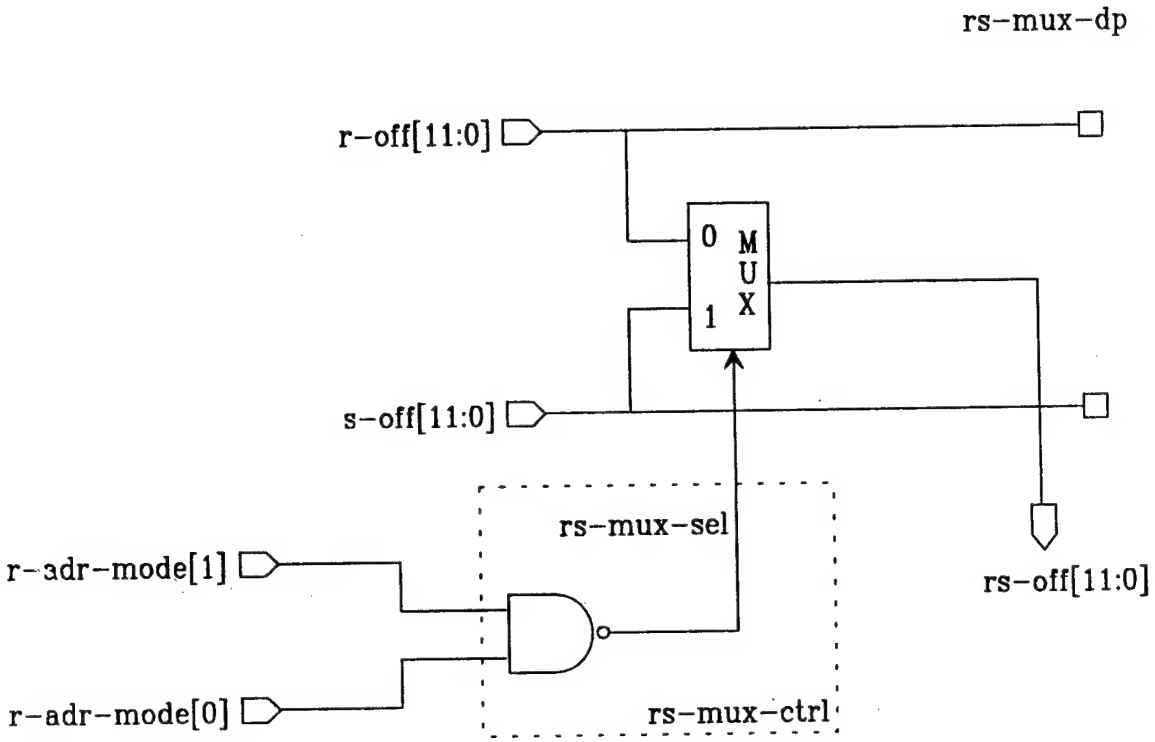
boot–ctrl



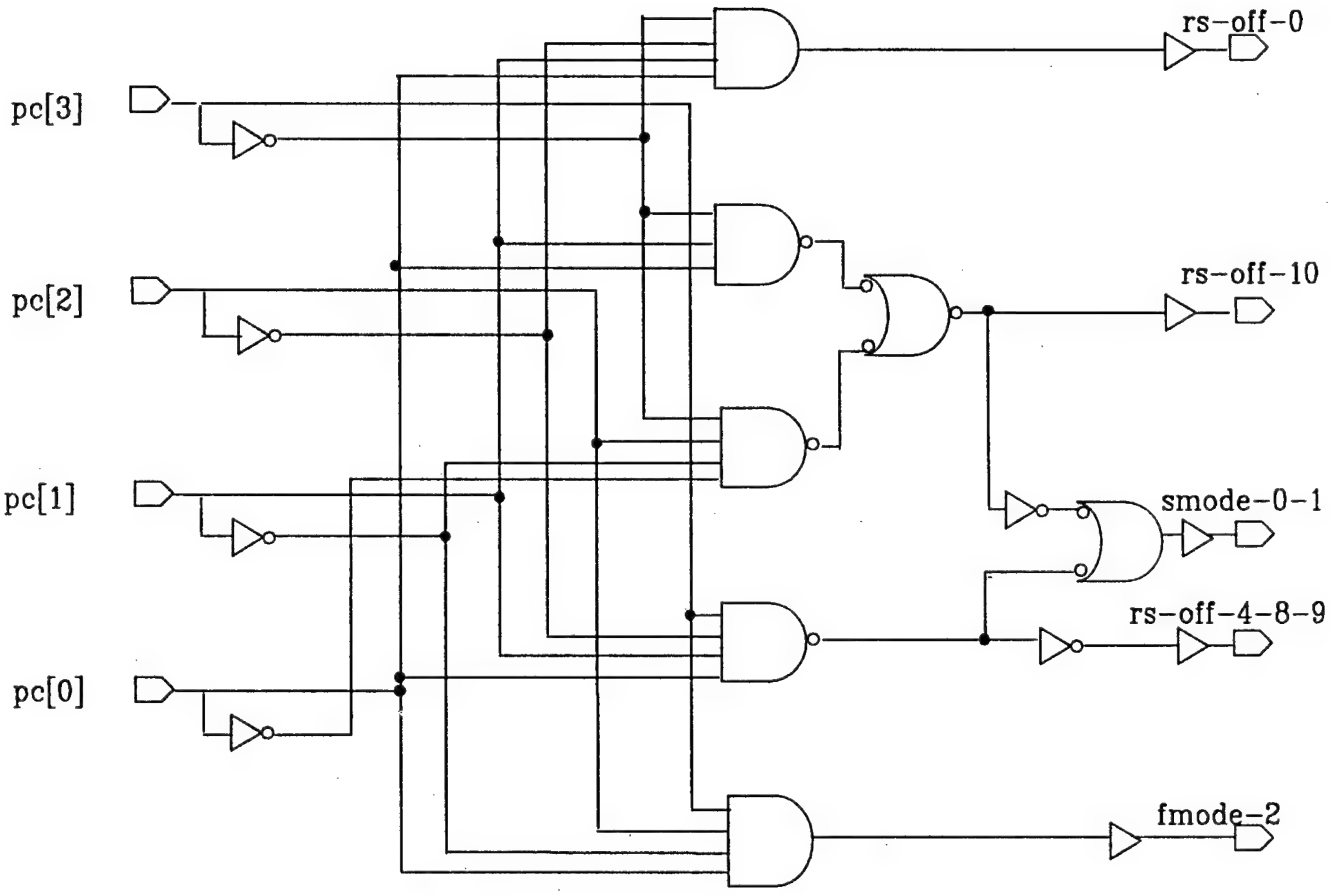
rf–off–mode–dp



rf–off–mode–mod


rs-mux-dp
r-off[11:0]
0
M
U
X
1
s-off[11:0]
rs-mux-sel
rs-off[11:0]
r-adr-mode[1]
r-adr-mode[0]
rs-mux-ctrl

rs-mux-mod



signals	drives
rs–off–0	rs–off–rom[0]
rs–off–10	rs–off–rom[10]
smode–0–1	s–mode–rom[1,0]
rs–off–4–8–9	rs–off–rom[9,8,4]
fmode–2	f–mode–rom[2]

boot–ctrl

6. Timing Diagrams

Timing diagrams for GT–VDAG are found in the GT–VIAG documentation.

7. Pin Description

Pin#	Loc.	Signal Name	Abbrev. Name	Pad Type	Strength	Timing
1	B1	S_eq_f_2	Seqf2	DATA OUT	DRVSPEED1	SB
2	C4	Ids_freeze	Ids_frz	DATA IN	NORMAL	VB
3	C2	RF[0]	RF_0	DATA IO	NORM,DRV1	W
4	C3	Freeze	Freeze	DATA IN	HIGH	VB
5	C1	Pc[2]	Pc_2	DATA IN	NORMAL	VB
6	D4	Pc[3]	Pc_3	DATA IN	NORMAL	VB
7	D2					
8	D3	Pc[1]	Pc_1	DATA IN	NORMAL	VB
9	F4					
10	G4	Pc[0]	Pc_0	DATA IN	NORMAL	VB
11	D1	Ids_eq_ods[0]	Idsods_0	DATA IN	NORMAL	VB
12	E4	Ids_eq_ods[1]	Idsods_1	DATA IN	NORMAL	VB
13	E1	RF[1]	RF_1	DATA IO	NORM,DRV1	W
14	E3	Ods_freeze	Ods_frz	DATA IN	NORMAL	VA
15	F2	RF[2]	RF_2	DATA IO	NORM,DRV1	W
16	E2	RF[3]	RF_3	DATA IO	NORM,DRV1	W
17	F1	VSS	VSS	VSS EDGE		
18	F3	VDD	VDD	VDD EDGE		
19	G1	VSS	VSS	VSS EDGE		
20	G3	RF[4]	RF_4	DATA IO	NORM,DRV1	W
21	H2	RF[5]	RF_5	DATA IO	NORM,DRV1	W
22	G2	RF[6]	RF_6	DATA IO	NORM,DRV1	W
23	H1	RF[7]	RF_7	DATA IO	NORM,DRV1	W
24	H4	RF[8]	RF_8	DATA IO	NORM,DRV1	W
25	J1	RF[9]	RF_9	DATA IO	NORM,DRV1	W
26	H3					
27	J2	RF[10]	RF_10	DATA IO	NORM,DRV1	W
28	H5	DAG_R_en	DAG_R_en	DATA IN	NORMAL	VB
29	J5	VDD	VDD	VDD CLOCK		
30	K1	VSS	VSS	VSS CLOCK		
31	J4	Clk	Clk	CLOCK		
32	K2	VDD	VDD	VDD EDGE		
33	J3	VSS	VSS	VSS EDGE		
34	L1	RF[11]	RF_11	DATA IO	NORM,DRV1	W
35	K3	RF[12]	RF_12	DATA IO	NORM,DRV1	W
36	M1	RF[13]	RF_13	DATA IO	NORM,DRV1	W
37	K4	RF[14]	RF_14	DATA IO	NORM,DRV1	W
38	N1	RF[15]	RF_15	DATA IO	NORM,DRV1	W
39	K5	RF[16]	RF_16	DATA IO	NORM,DRV1	W

40	M2	RF[17]	RF_17	DATA IO	NORM,DRV1	W
41	L3	RF[18]	RF_18	DATA IO	NORM,DRV1	W
42	P1	VDD	VDD	VDD EDGE		
43	L2	VSS	VSS	VSS EDGE		
44	R1	RF[19]	RF_19	DATA IO	NORM,DRV1	W
45	M3	RF[20]	RF_20	DATA IO	NORM,DRV1	W
46	M4	RF[23]	RF_23	DATA IO	NORM,DRV1	W
47	L4	RF[21]	RF_21	DATA IO	NORM,DRV1	W
48	P2	RF[24]	RF_24	DATA IO	NORM,DRV1	W
49	N2	RF[22]	RF_22	DATA IO	NORM,DRV1	W
50	T1					
51	N3	RF[26]	RF_26	DATA IO	NORM,DRV1	W
52	R2	RF[25]	RF_25	DATA IO	NORM,DRV1	W
53	N4	RF[28]	RF_28	DATA IO	NORM,DRV1	W
54	U1	RF[27]	RF_27	DATA IO	NORM,DRV1	W
55	P3	VDD	VDD	VDD EDGE		
56	T2	RF[29]	RF_29	DATA IO	NORM,DRV1	W
57	T3	VSS	VSS	VSS EDGE		
58	P4	VSS	VSS	VSS CORNER		
59	U2	RF[31]	RF_31	DATA IO	NORM,DRV1	W
60	R3	RF[30]	RF_30	DATA IO	NORM,DRV1	W
61	U3	RF_adr[1]	RFadr_1	DATA OUT	DRVSPEED1	W
62	T4	RF_adr[0]	RFadr_0	DATA OUT	DRVSPEED1	W
63	U4					
64	P5	RF_adr[2]	RFadr_2	DATA OUT	DRVSPEED1	W
65	P6	RF_adr[3]	RFadr_3	DATA OUT	DRVSPEED1	W
66	N7					
67	T5	RF_adr[4]	RFadr_4	DATA OUT	DRVSPEED1	W
68	R4	RF_adr[5]	RFadr_5	DATA OUT	DRVSPEED1	W
69	U5	RF_adr[6]	RFadr_6	DATA OUT	DRVSPEED1	W
70	R5	RF_adr[7]	RFadr_7	DATA OUT	DRVSPEED1	W
71	T6	RF_adr[9]	RFadr_9	DATA OUT	DRVSPEED1	W
72	R6	RF_adr[8]	RFadr_8	DATA OUT	DRVSPEED1	W
73	U6	VSS	VSS	VSS EDGE		
74	P7	VSS	VSS	VSS EDGE		
75	U7	VDD	VDD	VDD EDGE		
76	R7	RF_adr[10]	RFadr_10	DATA OUT	DRVSPEED1	W
77	T8	RF_adr[11]	RFadr_11	DATA OUT	DRVSPEED1	W
78	T7	RF_adr[12]	RFadr_12	DATA OUT	DRVSPEED1	W
79	U8	RF_adr[13]	RFadr_13	DATA OUT	DRVSPEED1	W
80	P8	RF_adr[14]	RFadr_14	DATA OUT	DRVSPEED1	W
81	U9	RF_adr[15]	RFadr_15	DATA OUT	DRVSPEED1	W
82	R8	RF_adr[16]	RFadr_16	DATA OUT	DRVSPEED1	W
83	T9	RF_adr[18]	RFadr_18	DATA OUT	DRVSPEED1	W
84	N8	RF_adr[17]	RFadr_17	DATA OUT	DRVSPEED1	W
85	N9	RF_adr[19]	RFadr_19	DATA OUT	DRVSPEED1	W
86	U10	VSS	VSS	VSS EDGE		
87	P9	VDD	VDD	VDD EDGE		
88	T10	RF_adr[20]	RFadr_20	DATA OUT	DRVSPEED1	W
89	R9	RF_adr[21]	RFadr_21	DATA OUT	DRVSPEED1	W
90	U11	RF_adr[22]	RFadr_22	DATA OUT	DRVSPEED1	W

91	R10	RF_adr[23]	RFadr_23	DATA OUT	DRVSPEED1	W
92	U12	RF_adr[24]	RFadr_24	DATA OUT	DRVSPEED1	W
93	N10	RF_adr[25]	RFadr_25	DATA OUT	DRVSPEED1	W
94	T12	RF_adr_mode[0]	RFmod_0	DATA IO	HIGH,DRV1	VB
95	P10	RF_adr_mode[1]	RFmod_1	DATA IO	HIGH,DRV1	VB
96	U13	RF_adr_mode[2]	RFmod_2	DATA IO	HIGH,DRV1	VB
97	T11	VSS	VSS	VSS EDGE		
98	T13	VDD	VDD	VDD EDGE		
99	R11	RF_adr_mode[3]	RFmod_3	DATA IO	HIGH,DRV1	VB
100	U14	RF_off[0]	RFoff_0	DATA IO	NORM,DRV1	VB
101	P11	RF_off[1]	RFoff_1	DATA IO	NORM,DRV1	VB
102	U15	RF_off[2]	RFoff_2	DATA IO	NORM,DRV1	VB
103	N11	RF_off[3]	RFoff_3	DATA IO	NORM,DRV1	VB
104	P12	VSS	VSS	VSS EDGE		
105	R12	RF_off[4]	RFoff_4	DATA IO	NORM,DRV1	VB
106	T15					
107	R13	RF_off[5]	RFoff_5	DATA IO	NORM,DRV1	VB
108	U16					
109	T14	RF_off[6]	RFoff_6	DATA IO	NORM,DRV1	VB
110	U17					
111	P13	RF_off[7]	RFoff_7	DATA IO	NORM,DRV1	VB
112	T16	VSS	VSS	VSS EDGE		
113	T17	VDD	VDD	VDD EDGE		
114	R14	VDD	VDD	VDD CORNER		
115	R16	RF_off[9]	RFoff_9	DATA IO	NORM,DRV1	VB
116	R15	RF_off[8]	RFoff_8	DATA IO	NORM,DRV1	VB
117	R17	RF_off[10]	RFoff_10	DATA IO	NORM,DRV1	VB
118	P14	VDD	VDD	VDD EDGE		
119	P16					
120	P15	RF_off[11]	RFoff_11	DATA IO	NORM,DRV1	VB
121	P17	RF_off[12]	RFoff_12	DATA IO	NORM,DRV1	VB
122	L14	RF_off[13]	RFoff_13	DATA IO	NORM,DRV1	VB
123	M14	RF_off[14]	RFoff_14	DATA IO	NORM,DRV1	VB
124	N14	RF_off[15]	RFoff_15	DATA IO	NORM,DRV1	VB
125	N17	RF_off[16]	RFoff_16	DATA IO	NORM,DRV1	VB
126	N15	VDD	VDD	VDD EDGE		
127	M16	VSS	VSS	VSS EDGE		
128	N16	VDD	VDD	VDD EDGE		
129	M17	RF_off[17]	RFoff_17	DATA IO	NORM,DRV1	VB
130	M15	RF_off[18]	RFoff_18	DATA IO	NORM,DRV1	VB
131	L17	RF_off[19]	RFoff_19	DATA IO	NORM,DRV1	VB
132	L15	RF_off[20]	RFoff_20	DATA IO	NORM,DRV1	VB
133	K16	RF_off[21]	RFoff_21	DATA IO	NORM,DRV1	VB
134	L16	RF_off[22]	RFoff_22	DATA IO	NORM,DRV1	VB
135	K17	RF_off[23]	RFoff_23	DATA IO	NORM,DRV1	VB
136	K14	RF_off[24]	RFoff_24	DATA IO	NORM,DRV1	VB
137	J17	RF_off[25]	RFoff_25	DATA IO	NORM,DRV1	VB
138	K15	S_off[0]	Soff_0	DATA IO	NORM,DRV1	VB
139	J16	S_off[1]	Soff_1	DATA IO	NORM,DRV1	VB
140	K13	S_off[2]	Soff_2	DATA IO	NORM,DRV1	VB
141	J13	S_off[3]	Soff_3	DATA IO	NORM,DRV1	VB

142	H17	VDD	VDD	VDD EDGE		
143	J14	VSS	VSS	VSS EDGE		
144	H16	S_off[4]	Soff_4	DATA IO	NORM,DRV1	VB
145	J15	S_off[5]	Soff_5	DATA IO	NORM,DRV1	VB
146	G17	S_off[6]	Soff_6	DATA IO	NORM,DRV1	VB
147	H15	S_off[7]	Soff_7	DATA IO	NORM,DRV1	VB
148	F17	S_off[8]	Soff_8	DATA IO	NORM,DRV1	VB
149	H14	VDD	VDD	VDD CORE		
150	F14	S_off[9]	Soff_9	DATA IO	NORM,DRV1	VB
151	H13	S_off[10]	Soff_10	DATA IO	NORM,DRV1	VB
152	F16	S_off[11]	Soff_11	DATA IO	NORM,DRV1	VB
153	G15	S_off[12]	Soff_12	DATA IO	NORM,DRV1	VB
154	D17	S_off[13]	Soff_13	DATA IO	NORM,DRV1	VB
155	G16	S_off[14]	Soff_14	DATA IO	NORM,DRV1	VB
156	C17	S_off[15]	Soff_15	DATA IO	NORM,DRV1	VB
157	F15	S_off[16]	Soff_16	DATA IO	NORM,DRV1	VB
158	D16	VDD	VDD	VDD EDGE		
159	G14	VSS	VSS	VSS EDGE		
160	F14	S_off[17]	Soff_17	DATA IO	NORM,DRV1	VB
161	E16	S_off[18]	Soff_18	DATA IO	NORM,DRV1	VB
162	B17					
163	E15	S_off[19]	Soff_19	DATA IO	NORM,DRV1	VB
164	C16					
165	E14	S_off[21]	Soff_21	DATA IO	NORM,DRV1	VB
166	A17	S_off[20]	Soff_20	DATA IO	NORM,DRV1	VB
167	D15	VDD	VDD	VDD EDGE		
168	B16	S_off[22]	Soff_22	DATA IO	NORM,DRV1	VB
169	B15	S_off[23]	Soff_23	DATA IO	NORM,DRV1	VB
170	D14	VSS	VSS	VSS EDGE		
171	A16	S_off[25]	Soff_25	DATA IO	NORM,DRV1	VB
172	C15	S_off[24]	Soff_24	DATA IO	NORM,DRV1	VB
173	A15	SF_adr[24]	SFadr_24	DATA OUT	DRVSPEED1	W
174	B14	SF_adr[25]	SFadr_25	DATA OUT	DRVSPEED1	W
175	A14					
176	D13	SF_adr[23]	SFadr_23	DATA OUT	DRVSPEED1	W
177	D12	SF_adr[22]	SFadr_22	DATA OUT	DRVSPEED1	W
178	E11	SF_adr[21]	SFadr_21	DATA OUT	DRVSPEED1	W
179	B13	SF_adr[20]	SFadr_20	DATA OUT	DRVSPEED1	W
180	C14	SF_adr[19]	SFadr_19	DATA OUT	DRVSPEED1	W
181	A13	SF_adr[18]	SFadr_18	DATA OUT	DRVSPEED1	W
182	C13	SF_adr[17]	SFadr_17	DATA OUT	DRVSPEED1	W
183	B12	VSS	VSS	VSS EDGE		
184	C2	VDD	VDD	VDD EDGE		
185	A12	SF_adr[16]	SFadr_16	DATA OUT	DRVSPEED1	W
186	D11	SF_adr[15]	SFadr_15	DATA OUT	DRVSPEED1	W
187	A11	SF_adr[14]	SFadr_14	DATA OUT	DRVSPEED1	W
188	C11	SF_adr[13]	SFadr_13	DATA OUT	DRVSPEED1	W
189	B10	SF_adr[12]	SFadr_12	DATA OUT	DRVSPEED1	W
190	B11	SF_adr[11]	SFadr_11	DATA OUT	DRVSPEED1	W
191	A10	SF_adr[10]	SFadr_10	DATA OUT	DRVSPEED1	W
192	D10	SF_adr[9]	SFadr_9	DATA OUT	DRVSPEED1	W

193	A9	SF_adr[8]	SFadr_8	DATA OUT	DRVSPEED1	W
194	C10	VSS	VSS	VSS EDGE		
195	B9	VDD	VDD	VDD EDGE		
196	E10	SF_adr[7]	SFadr_7	DATA OUT	DRVSPEED1	W
197	E9	SF_adr[6]	SFadr_6	DATA OUT	DRVSPEED1	W
198	A8	SF_adr[5]	SFadr_5	DATA OUT	DRVSPEED1	W
199	D9	SF_adr[4]	SFadr_4	DATA OUT	DRVSPEED1	W
200	B8	SF_adr[3]	SFadr_3	DATA OUT	DRVSPEED1	W
201	C9	SF_adr[2]	SFadr_2	DATA OUT	DRVSPEED1	W
202	A7	SF_adr[1]	SFadr_1	DATA OUT	DRVSPEED1	W
203	C8	SF_adr[0]	SFadr_0	DATA OUT	DRVSPEED1	W
204	A6	S_adr_mode[0]	Smode_0	DATA IO	HIGH,DRV1	VB
205	E8	S_adr_mode[1]	Smode_1	DATA IO	HIGH,DRV1	VB
206	B6	S_adr_mode[2]	Smode_2	DATA IO	HIGH,DRV1	VB
207	D8	S_adr_mode[3]	Smode_3	DATA IO	HIGH,DRV1	VB
208	A5	VSS	VSS	VSS EDGE		
209	B7	VDD	VDD	DD EDGE		
210	B5	N_reset	N_reset	DATA IN	HIGH	VB
211	C7	Flush	Flush	DATA IN	HIGH	VB
212	A4	Kernel_mode	Kmode	DATA IN	NORMAL	VB
213	D7	DAG_error	DAG_err	DATA OUT	DRVSPEED1	SB
214	D6	Booting	Booting	DATA IN	NORMAL	VB
215	E7	Guard	Guard	DATA IN	NORMAL	VB
216	A3	Inst_rd	Inst_rd	DATA IN	NORMAL	VB
217	C6	Inst_en	Inst_en	DATA IN	NORMAL	VB
218	B3					
219	C5	Valid_intr	Vld_intr	DATA IN	NORMAL	VB
220	A2					
221	B4	R_eq_f_1	Req_f1	DATA OUT	DRVSPEED1	VB
222	A1					
223	D5	S_eq_f_1	Seq_f1	DATA OUT	DRVSPEED1	VB
224	B2	R_eq_f_2	Req_f2	DATA OUT	DRVSPEED1	VB

8. Key Parameters

```
) Key Parameters for Chip /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag
) ================================================================================
)
) TIME = Fri Jan 25 11:09:00 1991
)
) ROUTE_VERSION = 8.00
) HEIGHT = 414.8 MILS
)    ( = 10535.9 u )
) WIDTH = 409.5 MILS
)    ( = 10401.3 u )
) ROUTED = 1 (0=NO,1=YES)
) TOTAL_WIRE_LENGTH = 1508101 MILS
)    ( = 38305765. u )
) CORE_AREA = 133448.0 SQUARE_MILS
)    ( = 86095313.2 u2 )
) PADRING_AREA = 36409.0 SQUARE_MILS
)    ( = 23489630. u2 )
```

```
) PAD_AREA = 32846.0 SQUARE_MILS
)     ( = 21190925. u2 )
) ROUTE_AREA = 83275.9 SQUARE_MILS
)     ( = 53726279. u2 )
) PERCENT_ROUTING_OF_CORE = 62 %
) PERCENT_ROUTING_OF_CHIP = 49 %
) PERCENT_CORE_OF_CHIP = 78 %
) PERCENT_PADRING_OF_CHIP = 21 %
) PERCENT_PAD_OF_PADRING = 90 %
)
) NETLIST_VERSION = 2.0
) NETLIST_EXISTS = 1 (0=NO,1=YES)
)
) PHASE_A_TIME = 46.1 NANOSECONDS
) PHASE_B_TIME = 46.6 NANOSECONDS
) SYMMETRIC_TIME = 94.0 NANOSECONDS
) NUMBER_OF_TRANSISTORS = 54569
) POWER_DISSIPATION = 991.97 MILLIWATTS_@5V_10MHZ
)
)
) ROUTE_ESTIMATE_LVL = 0
) FLAT_ROUTE = 0 (0=NO,1=YES)
) TECHNOLOGY_NAME = CMOS-1
) PACKAGE_SPECIFIED = 1 (0=NO,1=YES)
) PACKAGE_NAME = CPGA224f2
) FABLINE_NAME = HP2_CN10B
) COMPILER_TYPE = GCX
)
) FLOORPLAN_VERSION = 8.0
) BOND_PAD_CNT = 208
) HEIGHT_ESTIMATE = 360.40 MILS
)     ( = 9154.159 u )
) WIDTH_ESTIMATE = 361.31 MILS
)     ( = 9177.273 u )
) FUSED = 1 (0=NO,1=YES)
) FUSION_REQUIRED = 1 (0=NO,1=YES)
) PINOUT = 1 (0=NO,1=YES)
) PINOUT_REQUIRED = 1 (0=NO,1=YES)
) PLACED = 1 (0=NO,1=YES)
) PLACEMENT_REQUIRED = 1 (0=NO,1=YES)
)
)
) DOWN_BONDS_ALLOWED = 1 (0=NO,1=YES)
) PKG_PIN_COUNT = 224
) PKG_WELL_HEIGHT = 480.00 MILS
)     ( = 12192.00 u )
) PKG_WELL_WIDTH = 480.00 MILS
)     ( = 12192.00 u )
) AREA = 169860.6 SQUARE_MILS
)     ( = 109587262. u2 )
) OBJECT_TYPE = Chip
) AREA_PER_TRANSISTOR = 3.112767 SQUARE_MILS
)     ( = 2008.23278 u2 )
) PHYSICAL_IMPLEMENTATIONS_EXIST = 0 (0=NO,1=YES)
) CHECKPOINTS_EXIST = 0 (0=NO,1=YES)
) CAN_SET_FABLINE = 1 (0=NO,1=YES)
)
) Key Parameter Listing Complete
```

9. PADRING.033

OUTPUT RINGS REPORT Version 1

Noise contribution:(ma/nh) Speed0: 2.50 Speed1: 5.00 Speed2: 8.33 Speed3: 16.66
Limits: Maximum noise level: 100. Unacceptable level: 150

Combined power pads do not supply clean power to the core.
Their use is discouraged

Ring under analysis: VDD

PAD NAME	EDGE	SPEED	DRIVE TYPE	PAD SUPPLY	COMMENT
rf_pad[10]	EAST	1	CMOS	1	OK
rf_pad[9]	EAST	1	CMOS	1	OK
rf_pad[8]	EAST	1	CMOS	1	OK
rf_pad[7]	EAST	1	CMOS	1	OK
rf_pad[6]	EAST	1	CMOS	1	OK
rf_pad[5]	EAST	1	CMOS	1	OK
rf_pad[4]	EAST	1	CMOS	2	OK
ring_vdd[0]	EAST		POWER		
rf_pad[3]	EAST	1	CMOS	2	OK
rf_pad[2]	EAST	1	CMOS	2	OK
rf_pad[1]	EAST	1	CMOS	2	OK
rf_pad[0]	EAST	1	CMOS	2	OK
seqf2_pad	EAST	1	CMOS	2	OK
seqf1_pad	SOUTH	1	CMOS	2	OK
reqf2_pad	SOUTH	1	CMOS	2	OK
reqf1_pad	SOUTH	1	CMOS	2	OK
dag_error_pad	SOUTH	1	CMOS	2	OK
ring_vdd[9]	SOUTH		POWER		
s_mode_pad[3]	SOUTH	1	CMOS	2	OK
s_mode_pad[2]	SOUTH	1	CMOS	2	OK
s_mode_pad[1]	SOUTH	1	CMOS	3	OK
s_mode_pad[0]	SOUTH	1	CMOS	3	OK
s_adr_pad[0]	SOUTH	1	CMOS	2	OK
s_adr_pad[1]	SOUTH	1	CMOS	2	OK
s_adr_pad[2]	SOUTH	1	CMOS	2	OK
s_adr_pad[3]	SOUTH	1	CMOS	2	OK
s_adr_pad[4]	SOUTH	1	CMOS	2	OK
s_adr_pad[5]	SOUTH	1	CMOS	2	OK
s_adr_pad[6]	SOUTH	1	CMOS	1	OK
s_adr_pad[7]	SOUTH	1	CMOS	2	OK
ring_vdd[10]	SOUTH		POWER		
s_adr_pad[8]	SOUTH	1	CMOS	2	OK
s_adr_pad[9]	SOUTH	1	CMOS	2	OK
s_adr_pad[10]	SOUTH	1	CMOS	2	OK
s_adr_pad[11]	SOUTH	1	CMOS	2	OK
s_adr_pad[12]	SOUTH	1	CMOS	2	OK
s_adr_pad[13]	SOUTH	1	CMOS	2	OK
s_adr_pad[14]	SOUTH	1	CMOS	2	OK
s_adr_pad[15]	SOUTH	1	CMOS	2	OK
s_adr_pad[16]	SOUTH	1	CMOS	2	OK
ring_vdd[3]	SOUTH		POWER		
s_adr_pad[17]	SOUTH	1	CMOS	2	OK
s_adr_pad[18]	SOUTH	1	CMOS	1	OK
s_adr_pad[19]	SOUTH	1	CMOS	1	OK
s_adr_pad[20]	SOUTH	1	CMOS	1	OK

s_adr_pad[21]	SOUTH	1	CMOS	1	OK
s_adr_pad[22]	SOUTH	1	CMOS	1	OK
s_adr_pad[23]	SOUTH	1	CMOS	1	OK
s_adr_pad[24]	SOUTH	1	CMOS	1	OK
s_adr_pad[25]	SOUTH	1	CMOS	2	OK
s_off_pad[25]	SOUTH	1	CMOS	2	OK
s_off_pad[24]	SOUTH	1	CMOS	1	OK
s_off_pad[23]	SOUTH	1	CMOS	1	OK
s_off_pad[22]	WEST	1	CMOS	1	OK
s_off_pad[21]	WEST	1	CMOS	1	OK
s_off_pad[20]	WEST	1	CMOS	1	OK
s_off_pad[19]	WEST	1	CMOS	1	OK
s_off_pad[18]	WEST	1	CMOS	1	OK
s_off_pad[17]	WEST	1	CMOS	1	OK
ring_vdd[4]	WEST		POWER		
s_off_pad[16]	WEST	1	CMOS	1	OK
s_off_pad[15]	WEST	1	CMOS	1	OK
s_off_pad[14]	WEST	1	CMOS	1	OK
s_off_pad[13]	WEST	1	CMOS	2	OK
s_off_pad[12]	WEST	1	CMOS	2	OK
s_off_pad[11]	WEST	1	CMOS	2	OK
s_off_pad[10]	WEST	1	CMOS	2	OK
s_off_pad[9]	WEST	1	CMOS	2	OK
s_off_pad[8]	WEST	1	CMOS	2	OK
s_off_pad[7]	WEST	1	CMOS	2	OK
s_off_pad[6]	WEST	1	CMOS	1	OK
s_off_pad[5]	WEST	1	CMOS	1	OK
s_off_pad[4]	WEST	1	CMOS	1	OK
ring_vdd[8]	WEST		POWER		
s_off_pad[3]	WEST	1	CMOS	1	OK
s_off_pad[2]	WEST	1	CMOS	1	OK
s_off_pad[1]	WEST	1	CMOS	1	OK
s_off_pad[0]	WEST	1	CMOS	2	OK
rf_off_pad[25]	WEST	1	CMOS	2	OK
rf_off_pad[24]	WEST	1	CMOS	2	OK
rf_off_pad[23]	WEST	1	CMOS	2	OK
rf_off_pad[22]	WEST	1	CMOS	2	OK
rf_off_pad[21]	WEST	1	CMOS	2	OK
rf_off_pad[20]	WEST	1	CMOS	2	OK
rf_off_pad[19]	WEST	1	CMOS	2	OK
rf_off_pad[18]	WEST	1	CMOS	2	OK
rf_off_pad[17]	WEST	1	CMOS	3	OK
ring_vdd[7]	WEST		POWER		
rf_off_pad[16]	WEST	1	CMOS	3	OK
rf_off_pad[15]	WEST	1	CMOS	3	OK
rf_off_pad[14]	WEST	1	CMOS	3	OK
rf_off_pad[13]	WEST	1	CMOS	3	OK
rf_off_pad[12]	WEST	1	CMOS	3	OK
rf_off_pad[11]	WEST	1	CMOS	3	OK
rf_off_pad[10]	WEST	1	CMOS	3	OK
ring_vdd[6]	WEST		POWER		
rf_off_pad[9]	WEST	1	CMOS	3	OK
rf_off_pad[8]	WEST	1	CMOS	4	OK
corner_vdd	WEST		POWER		
rf_off_pad[7]	NORTH	1	CMOS	4	OK
rf_off_pad[6]	NORTH	1	CMOS	3	OK
rf_off_pad[5]	NORTH	1	CMOS	3	OK
rf_off_pad[4]	NORTH	1	CMOS	3	OK
rf_off_pad[3]	NORTH	1	CMOS	3	OK
rf_off_pad[2]	NORTH	1	CMOS	3	OK

rf_off_pad[1]	NORTH	1	CMOS	3	OK
rf_off_pad[0]	NORTH	1	CMOS	3	OK
rf_mode_pad[3]	NORTH	1	CMOS	3	OK
ring_vdd[5]	NORTH		POWER		
rf_mode_pad[2]	NORTH	1	CMOS	3	OK
rf_mode_pad[1]	NORTH	1	CMOS	2	OK
rf_mode_pad[0]	NORTH	1	CMOS	2	OK
rf_adr_pad[25]	NORTH	1	CMOS	2	OK
rf_adr_pad[24]	NORTH	1	CMOS	2	OK
rf_adr_pad[23]	NORTH	1	CMOS	2	OK
rf_adr_pad[22]	NORTH	1	CMOS	2	OK
rf_adr_pad[21]	NORTH	1	CMOS	2	OK
rf_adr_pad[20]	NORTH	1	CMOS	2	OK
ring_vdd[2]	NORTH		POWER		
rf_adr_pad[19]	NORTH	1	CMOS	3	OK
rf_adr_pad[17]	NORTH	1	CMOS	2	OK
rf_adr_pad[18]	NORTH	1	CMOS	2	OK
rf_adr_pad[16]	NORTH	1	CMOS	2	OK
rf_adr_pad[15]	NORTH	1	CMOS	2	OK
rf_adr_pad[14]	NORTH	1	CMOS	2	OK
rf_adr_pad[13]	NORTH	1	CMOS	2	OK
rf_adr_pad[12]	NORTH	1	CMOS	2	OK
rf_adr_pad[11]	NORTH	1	CMOS	2	OK
rf_adr_pad[10]	NORTH	1	CMOS	2	OK
ring_vdd[1]	NORTH		POWER		
rf_adr_pad[8]	NORTH	1	CMOS	1	OK
rf_adr_pad[9]	NORTH	1	CMOS	1	OK
rf_adr_pad[7]	NORTH	1	CMOS	2	OK
rf_adr_pad[6]	NORTH	1	CMOS	2	OK
rf_adr_pad[5]	NORTH	1	CMOS	2	OK
rf_adr_pad[4]	NORTH	1	CMOS	2	OK
rf_adr_pad[3]	NORTH	1	CMOS	2	OK
rf_adr_pad[2]	NORTH	1	CMOS	2	OK
rf_adr_pad[1]	NORTH	1	CMOS	2	OK
rf_adr_pad[0]	NORTH	1	CMOS	2	OK
rf_pad[31]	NORTH	1	CMOS	1	OK
rf_pad[30]	NORTH	1	CMOS	3	OK
ring_vdd[13]	EAST		POWER		
rf_pad[29]	EAST	1	CMOS	3	OK
rf_pad[28]	EAST	1	CMOS	3	OK
rf_pad[27]	EAST	1	CMOS	3	OK
rf_pad[26]	EAST	1	CMOS	3	OK
rf_pad[25]	EAST	1	CMOS	3	OK
rf_pad[22]	EAST	1	CMOS	3	OK
rf_pad[24]	EAST	1	CMOS	3	OK
rf_pad[21]	EAST	1	CMOS	3	OK
rf_pad[23]	EAST	1	CMOS	3	OK
rf_pad[20]	EAST	1	CMOS	3	OK
rf_pad[19]	EAST	1	CMOS	2	OK
ring_vdd[12]	EAST		POWER		
rf_pad[18]	EAST	1	CMOS	2	OK
rf_pad[17]	EAST	1	CMOS	2	OK
rf_pad[16]	EAST	1	CMOS	2	OK
rf_pad[15]	EAST	1	CMOS	2	OK
rf_pad[14]	EAST	1	CMOS	2	OK
rf_pad[13]	EAST	1	CMOS	2	OK
rf_pad[12]	EAST	1	CMOS	2	OK
rf_pad[11]	EAST	1	CMOS	2	OK
ring_vdd[11]	EAST		POWER		

```
This ring has 7 more VDD pads than it needs
 Ring under analysis: VSS

          PAD NAME        EDGE   SPEED DRIVE PAD      COMMENT
                                       TYPE  SUPPLY
-------------------------------------------------------------------------------

          rf_pad[10]      EAST     1  CMOS       2   OK
          rf_pad[9]       EAST     1  CMOS       2   OK
          rf_pad[8]       EAST     1  CMOS       2   OK
          rf_pad[7]       EAST     1  CMOS       2   OK
          rf_pad[6]       EAST     1  CMOS       2   OK
          rf_pad[5]       EAST     1  CMOS       2   OK
          rf_pad[4]       EAST     1  CMOS       3   OK
          ring_vss[11]    EAST        POWER
          ring_vss[10]    EAST        POWER
          rf_pad[3]       EAST     1  CMOS       3   OK
          rf_pad[2]       EAST     1  CMOS       3   OK
          rf_pad[1]       EAST     1  CMOS       3   OK
          rf_pad[0]       EAST     1  CMOS       3   OK
          seqf2_pad       EAST     1  CMOS       3   OK

          seqf1_pad       SOUTH    1  CMOS       3   OK
          reqf2_pad       SOUTH    1  CMOS       3   OK
          reqf1_pad       SOUTH    1  CMOS       3   OK
          dag_error_pad   SOUTH    1  CMOS       3   OK
          ring_vss[8]     SOUTH       POWER
          s_mode_pad[3]   SOUTH    1  CMOS       3   OK
          s_mode_pad[2]   SOUTH    1  CMOS       3   OK
          s_mode_pad[1]   SOUTH    1  CMOS       4   OK
          s_mode_pad[0]   SOUTH    1  CMOS       4   OK
          s_adr_pad[0]    SOUTH    1  CMOS       2   OK
          s_adr_pad[1]    SOUTH    1  CMOS       2   OK
          s_adr_pad[2]    SOUTH    1  CMOS       2   OK
          s_adr_pad[3]    SOUTH    1  CMOS       2   OK
          s_adr_pad[4]    SOUTH    1  CMOS       2   OK
          s_adr_pad[5]    SOUTH    1  CMOS       2   OK
          s_adr_pad[6]    SOUTH    1  CMOS       1   OK
          s_adr_pad[7]    SOUTH    1  CMOS       2   OK
          ring_vss[9]     SOUTH       POWER
          s_adr_pad[8]    SOUTH    1  CMOS       2   OK
          s_adr_pad[9]    SOUTH    1  CMOS       2   OK
          s_adr_pad[10]   SOUTH    1  CMOS       2   OK
          s_adr_pad[11]   SOUTH    1  CMOS       2   OK
          s_adr_pad[12]   SOUTH    1  CMOS       2   OK
          s_adr_pad[13]   SOUTH    1  CMOS       2   OK
          s_adr_pad[14]   SOUTH    1  CMOS       2   OK
          s_adr_pad[15]   SOUTH    1  CMOS       2   OK
          s_adr_pad[16]   SOUTH    1  CMOS       2   OK
          ring_vss[3]     SOUTH       POWER
          s_adr_pad[17]   SOUTH    1  CMOS       2   OK
          s_adr_pad[18]   SOUTH    1  CMOS       1   OK
          s_adr_pad[19]   SOUTH    1  CMOS       2   OK
          s_adr_pad[20]   SOUTH    1  CMOS       2   OK
          s_adr_pad[21]   SOUTH    1  CMOS       2   OK
          s_adr_pad[22]   SOUTH    1  CMOS       2   OK
          s_adr_pad[23]   SOUTH    1  CMOS       2   OK
          s_adr_pad[24]   SOUTH    1  CMOS       2   OK
          s_adr_pad[25]   SOUTH    1  CMOS       3   OK
          s_off_pad[25]   SOUTH    1  CMOS       3   OK
          s_off_pad[24]   SOUTH    1  CMOS       2   OK
```

```
s_off_pad[23]   SOUTH   1  CMOS      2   OK
corner_vss[1]   SOUTH      POWER

s_off_pad[22]   WEST    1  CMOS      2   OK
s_off_pad[21]   WEST    1  CMOS      2   OK
s_off_pad[20]   WEST    1  CMOS      2   OK
s_off_pad[19]   WEST    1  CMOS      2   OK
s_off_pad[18]   WEST    1  CMOS      2   OK
s_off_pad[17]   WEST    1  CMOS      2   OK
ring_vss[4]     WEST       POWER
s_off_pad[16]   WEST    1  CMOS      2   OK
s_off_pad[15]   WEST    1  CMOS      2   OK
s_off_pad[14]   WEST    1  CMOS      2   OK
s_off_pad[13]   WEST    1  CMOS      3   OK
s_off_pad[12]   WEST    1  CMOS      2   OK
s_off_pad[11]   WEST    1  CMOS      2   OK
s_off_pad[10]   WEST    1  CMOS      2   OK
s_off_pad[9]    WEST    1  CMOS      2   OK
s_off_pad[8]    WEST    1  CMOS      2   OK
s_off_pad[7]    WEST    1  CMOS      2   OK
s_off_pad[6]    WEST    1  CMOS      1   OK
s_off_pad[5]    WEST    1  CMOS      1   OK
s_off_pad[4]    WEST    1  CMOS      1   OK
ring_vss[7]     WEST       POWER
s_off_pad[3]    WEST    1  CMOS      1   OK
s_off_pad[2]    WEST    1  CMOS      1   OK
s_off_pad[1]    WEST    1  CMOS      1   OK
s_off_pad[0]    WEST    1  CMOS      2   OK
rf_off_pad[25]  WEST    1  CMOS      2   OK
rf_off_pad[24]  WEST    1  CMOS      2   OK
rf_off_pad[23]  WEST    1  CMOS      2   OK
rf_off_pad[22]  WEST    1  CMOS      2   OK
rf_off_pad[21]  WEST    1  CMOS      2   OK
rf_off_pad[20]  WEST    1  CMOS      2   OK
rf_off_pad[19]  WEST    1  CMOS      1   OK
rf_off_pad[18]  WEST    1  CMOS      1   OK
rf_off_pad[17]  WEST    1  CMOS      1   OK
ring_vss[6]     WEST       POWER
rf_off_pad[16]  WEST    1  CMOS      1   OK
rf_off_pad[15]  WEST    1  CMOS      1   OK
rf_off_pad[14]  WEST    1  CMOS      1   OK
rf_off_pad[13]  WEST    1  CMOS      1   OK
rf_off_pad[12]  WEST    1  CMOS      1   OK
rf_off_pad[11]  WEST    1  CMOS      1   OK
rf_off_pad[10]  WEST    1  CMOS      1   OK
rf_off_pad[9]   WEST    1  CMOS      1   OK
rf_off_pad[8]   WEST    1  CMOS      2   OK

rf_off_pad[7]   NORTH   1  CMOS      2   OK
rf_off_pad[6]   NORTH   1  CMOS      1   OK
rf_off_pad[5]   NORTH   1  CMOS      1   OK
rf_off_pad[4]   NORTH   1  CMOS      1   OK
rf_off_pad[3]   NORTH   1  CMOS      1   OK
rf_off_pad[2]   NORTH   1  CMOS      1   OK
rf_off_pad[1]   NORTH   1  CMOS      1   OK
rf_off_pad[0]   NORTH   1  CMOS      1   OK
rf_mode_pad[3]  NORTH   1  CMOS      2   OK
ring_vss[5]     NORTH      POWER
rf_mode_pad[2]  NORTH   1  CMOS      2   OK
rf_mode_pad[1]  NORTH   1  CMOS      2   OK
rf_mode_pad[0]  NORTH   1  CMOS      2   OK
rf_adr_pad[25]  NORTH   1  CMOS      2   OK
```

```
rf_adr_pad[24]  NORTH   1  CMOS      2   OK
rf_adr_pad[23]  NORTH   1  CMOS      2   OK
rf_adr_pad[22]  NORTH   1  CMOS      2   OK
rf_adr_pad[21]  NORTH   1  CMOS      2   OK
rf_adr_pad[20]  NORTH   1  CMOS      2   OK
ring_vss[1]     NORTH      POWER
rf_adr_pad[19]  NORTH   1  CMOS      3   OK
rf_adr_pad[17]  NORTH   1  CMOS      2   OK
rf_adr_pad[18]  NORTH   1  CMOS      2   OK
rf_adr_pad[16]  NORTH   1  CMOS      2   OK
rf_adr_pad[15]  NORTH   1  CMOS      2   OK
rf_adr_pad[14]  NORTH   1  CMOS      2   OK
rf_adr_pad[13]  NORTH   1  CMOS      2   OK
rf_adr_pad[12]  NORTH   1  CMOS      2   OK
rf_adr_pad[11]  NORTH   1  CMOS      2   OK
rf_adr_pad[10]  NORTH   1  CMOS      2   OK
ring_vss[0]     NORTH      POWER
rf_adr_pad[8]   NORTH   1  CMOS      1   OK
rf_adr_pad[9]   NORTH   1  CMOS      1   OK
rf_adr_pad[7]   NORTH   1  CMOS      2   OK
rf_adr_pad[6]   NORTH   1  CMOS      2   OK
rf_adr_pad[5]   NORTH   1  CMOS      2   OK
rf_adr_pad[4]   NORTH   1  CMOS      2   OK
rf_adr_pad[3]   NORTH   1  CMOS      2   OK
rf_adr_pad[2]   NORTH   1  CMOS      2   OK
rf_adr_pad[1]   NORTH   1  CMOS      2   OK
rf_adr_pad[0]   NORTH   1  CMOS      2   OK
rf_pad[31]      NORTH   1  CMOS      1   OK
rf_pad[30]      NORTH   1  CMOS      3   OK
corner_vss[0]   NORTH      POWER

rf_pad[29]      EAST    1  CMOS      3   OK
rf_pad[28]      EAST    1  CMOS      3   OK
rf_pad[27]      EAST    1  CMOS      3   OK
rf_pad[26]      EAST    1  CMOS      3   OK
rf_pad[25]      EAST    1  CMOS      3   OK
rf_pad[22]      EAST    1  CMOS      3   OK
rf_pad[24]      EAST    1  CMOS      3   OK
rf_pad[21]      EAST    1  CMOS      3   OK
rf_pad[23]      EAST    1  CMOS      3   OK
rf_pad[20]      EAST    1  CMOS      3   OK
rf_pad[19]      EAST    1  CMOS      2   OK
ring_vss[2]     EAST       POWER
rf_pad[18]      EAST    1  CMOS      2   OK
rf_pad[17]      EAST    1  CMOS      2   OK
rf_pad[16]      EAST    1  CMOS      2   OK
rf_pad[15]      EAST    1  CMOS      2   OK
rf_pad[14]      EAST    1  CMOS      2   OK
rf_pad[13]      EAST    1  CMOS      2   OK
rf_pad[12]      EAST    1  CMOS      2   OK
rf_pad[11]      EAST    1  CMOS      2   OK
ring_vss[12]    EAST       POWER

This ring has 7 more VSS pads than it needs
```

10. Power Dissipation

```
) Total power consumption (5.5V, 0 DegC 50pf/out_pad):
)       DC:         27.39mW [27.39(core)+0.00(ring)]
)       AC@10MHz:   946.23mW [265.62(core)+680.61(ring)]
```

11. Simulation Setup Files

11.1. designinit.080

```
func designinit {
            toggle /Clk 0 '(0 5 10)
            tag /Clk step both
            tag /Clk cycle rising
                        }
```

12. Timing Setup Files

12.1. cl_out_room.040

```
LABEL Clock time, output delay -- Room Temp
TEMP_VOLT 62 5.00
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Clk
INPUT Booting 1 0 14.70 0.00 0.00 0.00
INPUT DAG_R_en 1 0 59.70 0.00 9.70 0.00
INPUT DAG_R_en 0 1 27.50 0.00 0.00 0.00
INPUT Flush 1 0 38.50 0.00 0.00 0.00
INPUT Freeze 1 0 45.70 0.00 0.00 0.00
INPUT Freeze 0 1 27.70 0.00 0.00 0.00
INPUT Guard 1 0 78.50 0.00 0.00 0.00
INPUT Guard 0 1 30.20 0.00 0.00 0.00
INPUT Ids_eq_ods_1 1 0 20.20 0.00 0.00 0.00
INPUT Ids_eq_ods_2 1 0 21.10 0.00 0.00 0.00
INPUT Ids_freeze 1 0 16.60 0.00 0.00 0.00
INPUT Ids_freeze 0 1 22.90 0.00 0.00 0.00
INPUT Inst_en 0 1 12.90 0.00 0.00 0.00
INPUT Kernel_mode 1 0 26.60 0.00 0.00 0.00
INPUT Inst_rd 1 0 52.70 0.00 0.00 0.00
INPUT Inst_rd 0 1 2.70 0.00 0.00 0.00
INPUT N_reset 1 0 23.10 0.00 0.00 0.00
INPUT Ods_freeze 1 0 40.50 0.00 0.00 0.00
INPUT Ods_freeze 0 1 16.60 0.00 0.00 0.00
INPUT Pc[0] 1 0 65.00 0.00 15.00 0.00
INPUT Pc[1] 1 0 65.00 0.00 15.00 0.00
INPUT Pc[2] 1 0 65.00 0.00 15.00 0.00
INPUT Pc[3] 1 0 65.00 0.00 15.00 0.00
INPUT Pc[0] 0 1 15.00 0.00 0.00 0.00
INPUT Pc[1] 0 1 15.00 0.00 0.00 0.00
INPUT Pc[2] 0 1 15.00 0.00 0.00 0.00
INPUT Pc[3] 0 1 15.00 0.00 0.00 0.00
INPUT Valid_intr 1 0 29.70 0.00 0.00 0.00
INPUT RF[0] 1 0 40.50 0.00 0.00 0.00
INPUT RF[1] 1 0 40.50 0.00 0.00 0.00
INPUT RF[2] 1 0 40.50 0.00 0.00 0.00
INPUT RF[3] 1 0 40.50 0.00 0.00 0.00
INPUT RF[4] 1 0 40.50 0.00 0.00 0.00
INPUT RF[5] 1 0 40.50 0.00 0.00 0.00
INPUT RF[6] 1 0 40.50 0.00 0.00 0.00
INPUT RF[7] 1 0 40.50 0.00 0.00 0.00
INPUT RF[8] 1 0 40.50 0.00 0.00 0.00
INPUT RF[9] 1 0 40.50 0.00 0.00 0.00
INPUT RF[10] 1 0 40.50 0.00 0.00 0.00
```

```
INPUT RF[11] 1 0 40.50 0.00 0.00 0.00
INPUT RF[12] 1 0 40.50 0.00 0.00 0.00
INPUT RF[13] 1 0 40.50 0.00 0.00 0.00
INPUT RF[14] 1 0 40.50 0.00 0.00 0.00
INPUT RF[15] 1 0 40.50 0.00 0.00 0.00
INPUT RF[16] 1 0 40.50 0.00 0.00 0.00
INPUT RF[17] 1 0 40.50 0.00 0.00 0.00
INPUT RF[18] 1 0 40.50 0.00 0.00 0.00
INPUT RF[19] 1 0 40.50 0.00 0.00 0.00
INPUT RF[20] 1 0 40.50 0.00 0.00 0.00
INPUT RF[21] 1 0 40.50 0.00 0.00 0.00
INPUT RF[22] 1 0 40.50 0.00 0.00 0.00
INPUT RF[23] 1 0 40.50 0.00 0.00 0.00
INPUT RF[24] 1 0 40.50 0.00 0.00 0.00
INPUT RF[25] 1 0 40.50 0.00 0.00 0.00
INPUT RF[26] 1 0 40.50 0.00 0.00 0.00
INPUT RF[27] 1 0 40.50 0.00 0.00 0.00
INPUT RF[28] 1 0 40.50 0.00 0.00 0.00
INPUT RF[29] 1 0 40.50 0.00 0.00 0.00
INPUT RF[0] 0 1 43.60 0.00 0.00 0.00
INPUT RF[1] 0 1 43.60 0.00 0.00 0.00
INPUT RF[2] 0 1 43.60 0.00 0.00 0.00
INPUT RF[3] 0 1 43.60 0.00 0.00 0.00
INPUT RF[4] 0 1 43.60 0.00 0.00 0.00
INPUT RF[5] 0 1 43.60 0.00 0.00 0.00
INPUT RF[6] 0 1 43.60 0.00 0.00 0.00
INPUT RF[7] 0 1 43.60 0.00 0.00 0.00
INPUT RF[8] 0 1 43.60 0.00 0.00 0.00
INPUT RF[9] 0 1 43.60 0.00 0.00 0.00
INPUT RF[10] 0 1 43.60 0.00 0.00 0.00
INPUT RF[11] 0 1 43.60 0.00 0.00 0.00
INPUT RF[12] 0 1 43.60 0.00 0.00 0.00
INPUT RF[13] 0 1 43.60 0.00 0.00 0.00
INPUT RF[14] 0 1 43.60 0.00 0.00 0.00
INPUT RF[15] 0 1 43.60 0.00 0.00 0.00
INPUT RF[16] 0 1 43.60 0.00 0.00 0.00
INPUT RF[17] 0 1 43.60 0.00 0.00 0.00
INPUT RF[18] 0 1 43.60 0.00 0.00 0.00
INPUT RF[19] 0 1 43.60 0.00 0.00 0.00
INPUT RF[20] 0 1 43.60 0.00 0.00 0.00
INPUT RF[21] 0 1 43.60 0.00 0.00 0.00
INPUT RF[22] 0 1 43.60 0.00 0.00 0.00
INPUT RF[23] 0 1 43.60 0.00 0.00 0.00
INPUT RF[24] 0 1 43.60 0.00 0.00 0.00
INPUT RF[25] 0 1 43.60 0.00 0.00 0.00
INPUT RF[26] 0 1 43.60 0.00 0.00 0.00
INPUT RF[27] 0 1 43.60 0.00 0.00 0.00
INPUT RF[28] 0 1 43.60 0.00 0.00 0.00
INPUT RF[29] 0 1 43.60 0.00 0.00 0.00
INPUT RF_adr_mode[0] 1 0 40.00 0.00 0.00 0.00
INPUT RF_adr_mode[1] 1 0 40.00 0.00 0.00 0.00
INPUT RF_adr_mode[2] 1 0 40.00 0.00 0.00 0.00
INPUT RF_adr_mode[3] 1 0 40.00 0.00 0.00 0.00
INPUT RF_adr_mode[0] 0 1 40.00 0.00 0.00 0.00
INPUT RF_adr_mode[1] 0 1 40.00 0.00 0.00 0.00
INPUT RF_adr_mode[2] 0 1 40.00 0.00 0.00 0.00
INPUT RF_adr_mode[3] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[0] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[1] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[2] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[3] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[4] 1 0 25.00 0.00 0.00 0.00
```

```
INPUT RF_off[5] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[6] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[7] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[8] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[9] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[10] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[11] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[12] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[13] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[14] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[15] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[16] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[17] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[18] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[19] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[20] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[21] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[22] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[23] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[24] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[25] 1 0 25.00 0.00 0.00 0.00
INPUT RF_off[0] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[1] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[2] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[3] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[4] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[5] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[6] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[7] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[8] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[9] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[10] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[11] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[12] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[13] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[14] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[15] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[16] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[17] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[18] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[19] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[20] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[21] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[22] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[23] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[24] 0 1 40.00 0.00 0.00 0.00
INPUT RF_off[40] 0 1 25.00 0.00 0.00 0.00
INPUT S_adr_mode[0] 0 1 40.00 0.00 0.00 0.00
INPUT S_adr_mode[1] 0 1 40.00 0.00 0.00 0.00
INPUT S_adr_mode[2] 0 1 40.00 0.00 0.00 0.00
INPUT S_adr_mode[3] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[0] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[1] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[2] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[3] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[4] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[5] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[6] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[7] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[8] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[9] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[10] 0 1 40.00 0.00 0.00 0.00
```

```
INPUT S_off[11] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[12] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[13] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[14] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[15] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[16] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[17] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[18] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[19] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[20] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[21] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[22] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[23] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[24] 0 1 40.00 0.00 0.00 0.00
INPUT S_off[40] 0 1 25.00 0.00 0.00 0.00
NO_PROP Booting 2
NO_PROP Flush 2
NO_PROP Ids_eq_ods_1 2
NO_PROP Ids_eq_ods_2 2
NO_PROP Kernel_mode 2
NO_PROP N_reset 2
NO_PROP Valid_intr 2
IGNORE_PATH rf_pad[0]/r_out rf_pad[0]/rf
IGNORE_PATH rf_pad[1]/r_out rf_pad[1]/rf
IGNORE_PATH rf_pad[2]/r_out rf_pad[2]/rf
IGNORE_PATH rf_pad[3]/r_out rf_pad[3]/rf
IGNORE_PATH rf_pad[4]/r_out rf_pad[4]/rf
IGNORE_PATH rf_pad[5]/r_out rf_pad[5]/rf
IGNORE_PATH rf_pad[6]/r_out rf_pad[6]/rf
IGNORE_PATH rf_pad[7]/r_out rf_pad[7]/rf
IGNORE_PATH rf_pad[8]/r_out rf_pad[8]/rf
IGNORE_PATH rf_pad[9]/r_out rf_pad[9]/rf
IGNORE_PATH rf_pad[10]/r_out rf_pad[10]/rf
IGNORE_PATH rf_pad[11]/r_out rf_pad[11]/rf
IGNORE_PATH rf_pad[12]/r_out rf_pad[12]/rf
IGNORE_PATH rf_pad[13]/r_out rf_pad[13]/rf
IGNORE_PATH rf_pad[14]/r_out rf_pad[14]/rf
IGNORE_PATH rf_pad[15]/r_out rf_pad[15]/rf
IGNORE_PATH rf_pad[16]/r_out rf_pad[16]/rf
IGNORE_PATH rf_pad[17]/r_out rf_pad[17]/rf
IGNORE_PATH rf_pad[18]/r_out rf_pad[18]/rf
IGNORE_PATH rf_pad[19]/r_out rf_pad[19]/rf
IGNORE_PATH rf_pad[20]/r_out rf_pad[20]/rf
IGNORE_PATH rf_pad[21]/r_out rf_pad[21]/rf
IGNORE_PATH rf_pad[22]/r_out rf_pad[22]/rf
IGNORE_PATH rf_pad[23]/r_out rf_pad[23]/rf
IGNORE_PATH rf_pad[24]/r_out rf_pad[24]/rf
IGNORE_PATH rf_pad[25]/r_out rf_pad[25]/rf
IGNORE_PATH rf_pad[26]/r_out rf_pad[26]/rf
IGNORE_PATH rf_pad[27]/r_out rf_pad[27]/rf
IGNORE_PATH rf_pad[28]/r_out rf_pad[28]/rf
IGNORE_PATH rf_pad[29]/r_out rf_pad[29]/rf
IGNORE_PATH rf_pad[0]/dag_r_dis rf_pad[0]/rf
IGNORE_PATH rf_pad[1]/dag_r_dis rf_pad[1]/rf
IGNORE_PATH rf_pad[2]/dag_r_dis rf_pad[2]/rf
IGNORE_PATH rf_pad[3]/dag_r_dis rf_pad[3]/rf
IGNORE_PATH rf_pad[4]/dag_r_dis rf_pad[4]/rf
IGNORE_PATH rf_pad[5]/dag_r_dis rf_pad[5]/rf
IGNORE_PATH rf_pad[6]/dag_r_dis rf_pad[6]/rf
IGNORE_PATH rf_pad[7]/dag_r_dis rf_pad[7]/rf
IGNORE_PATH rf_pad[8]/dag_r_dis rf_pad[8]/rf
IGNORE_PATH rf_pad[9]/dag_r_dis rf_pad[9]/rf
```

```
IGNORE_PATH rf_pad[10]/dag_r_dis rf_pad[10]/rf
IGNORE_PATH rf_pad[11]/dag_r_dis rf_pad[11]/rf
IGNORE_PATH rf_pad[12]/dag_r_dis rf_pad[12]/rf
IGNORE_PATH rf_pad[13]/dag_r_dis rf_pad[13]/rf
IGNORE_PATH rf_pad[14]/dag_r_dis rf_pad[14]/rf
IGNORE_PATH rf_pad[15]/dag_r_dis rf_pad[15]/rf
IGNORE_PATH rf_pad[16]/dag_r_dis rf_pad[16]/rf
IGNORE_PATH rf_pad[17]/dag_r_dis rf_pad[17]/rf
IGNORE_PATH rf_pad[18]/dag_r_dis rf_pad[18]/rf
IGNORE_PATH rf_pad[19]/dag_r_dis rf_pad[19]/rf
IGNORE_PATH rf_pad[20]/dag_r_dis rf_pad[20]/rf
IGNORE_PATH rf_pad[21]/dag_r_dis rf_pad[21]/rf
IGNORE_PATH rf_pad[22]/dag_r_dis rf_pad[22]/rf
IGNORE_PATH rf_pad[23]/dag_r_dis rf_pad[23]/rf
IGNORE_PATH rf_pad[24]/dag_r_dis rf_pad[24]/rf
IGNORE_PATH rf_pad[25]/dag_r_dis rf_pad[25]/rf
IGNORE_PATH rf_pad[26]/dag_r_dis rf_pad[26]/rf
IGNORE_PATH rf_pad[27]/dag_r_dis rf_pad[27]/rf
IGNORE_PATH rf_pad[28]/dag_r_dis rf_pad[28]/rf
IGNORE_PATH rf_pad[29]/dag_r_dis rf_pad[29]/rf
IGNORE_PATH rf_mode_pad[0]/rfadr_mode_ou rf_mode_pad[0]/rf_adr_mode
IGNORE_PATH rf_mode_pad[1]/rfadr_mode_ou rf_mode_pad[1]/rf_adr_mode
IGNORE_PATH rf_mode_pad[2]/rfadr_mode_ou rf_mode_pad[2]/rf_adr_mode
IGNORE_PATH rf_mode_pad[3]/rfadr_mode_ou rf_mode_pad[3]/rf_adr_mode
IGNORE_PATH s_mode_pad[0]/s_adr_mode_ou s_mode_pad[0]/s_adr_mode_in
IGNORE_PATH s_mode_pad[1]/s_adr_mode_ou s_mode_pad[1]/s_adr_mode_in
IGNORE_PATH s_mode_pad[2]/s_adr_mode_ou s_mode_pad[2]/s_adr_mode_in
IGNORE_PATH s_mode_pad[3]/s_adr_mode_ou s_mode_pad[3]/s_adr_mode_in
IGNORE_PATH rf_mode_pad[0]/inst_dis rf_mode_pad[0]/rf_adr_mode
IGNORE_PATH rf_mode_pad[1]/inst_dis rf_mode_pad[1]/rf_adr_mode
IGNORE_PATH rf_mode_pad[2]/inst_dis rf_mode_pad[2]/rf_adr_mode
IGNORE_PATH rf_mode_pad[3]/inst_dis rf_mode_pad[3]/rf_adr_mode
IGNORE_PATH s_mode_pad[0]/inst_dis s_mode_pad[0]/s_adr_mode_in
IGNORE_PATH s_mode_pad[1]/inst_dis s_mode_pad[1]/s_adr_mode_in
IGNORE_PATH s_mode_pad[2]/inst_dis s_mode_pad[2]/s_adr_mode_in
IGNORE_PATH s_mode_pad[3]/inst_dis s_mode_pad[3]/s_adr_mode_in
```

12.2. cl_out_hot

```
LABEL Clock time, output delay -- Max T, Min V
TEMP_VOLT 112 4.50
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Clk
```

The rest of this file is identical to cl_out_room's INPUT and IGNORE_PATH statements.

12.3. set_room.040

```
LABEL Setup/Hold time, Violations -- Room Temp
TEMP_VOLT 62 5.00
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Clk
```

The rest of this file is identical to cl_out_room's INPUT and IGNORE_PATH statements.

12.4. set_hot.040

```
LABEL Setup/Hold time, Violations -- Max T, Min V
TEMP_VOLT 112 4.50
```

```
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Clk

The rest of this file is identical to cl_out_room's INPUT and IGNORE_PATH statements.
```

12.5. clock_output.040

```
LABEL Clock time, output delay
TEMP_VOLT 75 5.00
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Clk

The rest of this file is identical to cl_out_room's INPUT and IGNORE_PATH statements.
```

12.6. setup_hold.040

```
LABEL Setup/Hold time, Violations
TEMP_VOLT 75 5.00
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Clk

The rest of this file is identical to cl_out_room's INPUT and IGNORE_PATH statements.
```

13. Timing Reports

13.1. TYPICAL, 75 deg C, 5.0 V

```
 ********************************************************************************
              Genesil Version v8.0.2 -- Thu Jan 24 14:15:16 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
 ********************************************************************************
CLOCK REPORT MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: TYPICAL
  Junction Temperature:75 deg C         Voltage:5.00v
  External Clock: Clk
 Included setup files:
  #0  clock_output           (Clock time, output delay)
--------------------------------------------------------------------------------
                           CLOCK TIMES (minimum)
Phase 1 High:    46.1   ns             Phase 2 High:    46.6   ns
            ----------                              ----------
Cycle (from Ph1):    94.0   ns        Cycle (from Ph2):    81.9   ns
                  ----------                              ----------
Minimum Cycle Time:    94.0   ns      Symmetric Cycle Time:     94.0   ns
                     ----------                              ----------
--------------------------------------------------------------------------------
                           CLOCK WORST CASE PATHS
Minimum Phase 1 high time is    46.1   ns set by:
                           ----------
  ** Clock delay: 2.0ns (48.1-46.1)
   Node                          Cumulative Delay      Transition
   <dr_gen/critical_rl/(internal)      48.1                rise
   f_adr_gen/critical_rl/mnz           46.8                fall
   <en/critical_rl/f_boot_mode[1]      45.6                rise
   <n/critical_rl/f_boot_mode[1]'      45.1                rise
```

```
   <adr_gen/critical_rl/n_mode[1]      44.7                fall
   <en/critical_rl/rf_adr_mode[1]      44.4                rise
   rf_mode_pad[1]/rf_adr_mode          44.4                rise
   rf_mode_pad[1]/rf_adr_mode'         42.0                rise
   RF_adr_mode[1]                      40.0                rise

Minimum Phase 2 high time is    46.6   ns set by:
                           ----------
  ** Clock delay: 1.7ns (48.4-46.6)
   Node                             Cumulative Delay      Transition
   <rlas_mod/frlas_mux/(internal)      48.4                fall
   frlas_mod/frlas_mux/rf[0]           47.5                rise
   rf_pad[0]/rf                        47.5                rise
   rf_pad[0]/rf'                       45.6                rise
   RF[0]                               43.6                rise

Minimum cycle time (from Ph1) is   94.0    ns set by:
                           ----------
  ** Clock delay: 3.4ns (97.5-94.0)
   Node                             Cumulative Delay      Transition
   adr_ptr_mod/adr_ptr_dp/8            97.5                fall
   *<tr_mod/adr_ptr_dp/(internal)      96.3                rise
   <_mod/adr_ptr_dp/ld_restore_ap      96.1                fall
   <od/adr_ptr_ctrl/ld_restore_ap      96.1                fall
   <d/adr_ptr_ctrl/ld_restore_ap'      95.1                fall
   <d/adr_ptr_ctrl/ld_rs_ap_no_fr      94.2                fall
   <tr_mod/adr_ptr_ctrl/change_ap      92.9                fall
   <r_mod/adr_ptr_ctrl/change_ap'      92.8                fall
   <r_mod/adr_ptr_ctrl/ld_inc_dec      91.7                fall
   <tr_mod/adr_ptr_ctrl/decrement      90.1                fall
   <r_mod/adr_ptr_ctrl/decrement'      88.6                fall
   <_ptr_mod/adr_ptr_ctrl/dec_mux      87.5                fall
   <ptr_mod/adr_ptr_ctrl/dec_mux'      87.4                fall
   <r_mod/adr_ptr_ctrl/decr_ap_in      86.4                fall
   <_mod/adr_ptr_ctrl/decr_ap_in'      86.1                fall
   <_mod/adr_ptr_ctrl/n_res_fl_fr      85.0                fall
   <mod/adr_ptr_ctrl/n_res_fl_fr'      85.0                fall
   <r_ptr_mod/adr_ptr_ctrl/freeze      83.8                rise
   <mod/adr_ptr_ctrl/n_freeze_buf      83.3                fall
   <od/adr_ptr_ctrl/n_freeze_buf'      83.2                fall
   <ptr_mod/adr_ptr_ctrl/n_freeze      82.3                fall
   freeze_pad/n_freeze                 82.3                fall
   freeze_pad/n_freeze'                79.2                fall
   Freeze                              77.7                rise

Minimum cycle time (from Ph2) is   81.9    ns set by:
                           ----------
  ** Clock delay: 3.2ns (85.1-81.9)
   Node                             Cumulative Delay      Transition
   error_mod/error_ff/s_eq_f_2         85.1                rise
   odc_rf_mod/odc_mux/odc_out[1]       85.1                rise
   odc_rf_mod/odc_mux/odc_out[1]'      84.4                rise
   <_rf_mod/odc_mux/INTER0_ST1[1]      82.6                rise
   odc_rf_mod/odc_mux/odc_in[1]        81.6                rise
   odc_rf_mod/odc_ctrl/s2              81.6                rise
   odc_rf_mod/odc_ctrl/s2'             81.1                rise
   <rf_mod/odc_ctrl/GB.LP.NNZ5fN2      80.9                fall
   odc_rf_mod/odc_ctrl/s2_int          80.6                rise
   odc_rf_mod/odc_rf_dp/s_eq_f_2       80.6                rise
   odc_rf_mod/odc_rf_dp/s_eq_f_2'      80.3                rise
   odc_rf_mod/odc_rf_dp/s_adr[25]      77.6                rise
   s_adr_gen/super_dp/adr[25]          77.6                rise
```

```
   s_adr_gen/super_dp/adr[25]'          77.2              rise
   <_gen/super_dp/ea_tpap_OUT[25]       75.1              rise
   <adr_gen/super_dp/no_tp_ST2[2]       58.7              fall
   <_gen/super_dp/eff_adr1_OUT[2]       57.8              fall
   <_gen/super_dp/eff_adr1_IN1[0]       53.1              fall
   <dr_gen/super_dp/mode_not_zero       50.8              fall
   <gen/critical_rl/mode_not_zero       50.8              fall
   <en/critical_rl/mode_not_zero'       50.0              fall
   *<r_gen/critical_rl/(internal)       48.4              fall
   s_adr_gen/critical_rl/mnz            47.2              fall
   s_adr_gen/critical_rl/mode[0]        45.8              rise
   s_adr_gen/critical_rl/mode[0]'       45.5              rise
   </critical_rl/s_adr_mode_in[0]       44.3              rise
   s_mode_pad[0]/s_adr_mode_in          44.3              rise
   s_mode_pad[0]/s_adr_mode_in'         42.0              rise
   S_adr_mode[0]                        40.0              rise
-------------------------------------------------------------------------------
 *******************************************************************************
             Genesil Version v8.0.2 -- Thu Jan 24 14:15:21 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
*******************************************************************************
OUTPUT DELAY MODE
-------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: TYPICAL
  Junction Temperature:75 deg C         Voltage:5.00v
  External Clock: Clk
 Included setup files:
  #0  clock_output           (Clock time, output delay)
-------------------------------------------------------------------------------
                              OUTPUT DELAYS (ns)
Output                    Ph1(r) Delay      Ph2(r) Delay      Loading(pf)
                          Min      Max      Min      Max
DAG_Error                 16.2     19.2     ---      ---      50.00   PATH
RF[0]                     13.9     89.3     38.9     39.3     50.00   PATH
RF[10]                    13.4     89.3     38.9     39.3     50.00   PATH
RF[11]                    13.3     89.3     38.9     39.3     50.00   PATH
RF[12]                    13.4     89.3     38.9     39.3     50.00   PATH
RF[13]                    15.0     89.3     38.9     39.3     50.00   PATH
RF[14]                    15.0     89.3     38.9     39.3     50.00   PATH
RF[15]                    15.0     89.3     38.9     39.3     50.00   PATH
RF[16]                    15.0     89.3     38.9     39.3     50.00   PATH
RF[17]                    15.4     89.3     38.9     39.3     50.00   PATH
RF[18]                    16.2     89.3     38.9     39.3     50.00   PATH
RF[19]                    16.1     89.3     38.9     39.3     50.00   PATH
RF[1]                     13.7     89.3     38.9     39.3     50.00   PATH
RF[20]                    16.3     89.3     38.9     39.3     50.00   PATH
RF[21]                    16.3     89.3     38.9     39.3     50.00   PATH
RF[22]                    15.6     89.3     38.9     39.3     50.00   PATH
RF[23]                    16.2     89.3     38.9     39.3     50.00   PATH
RF[24]                    16.2     89.3     38.9     39.3     50.00   PATH
RF[25]                    16.2     89.3     38.9     39.3     50.00   PATH
RF[26]                    16.8     89.3     38.9     39.3     50.00   PATH
RF[27]                    16.8     89.3     38.9     39.3     50.00   PATH
RF[28]                    16.7     89.3     38.9     39.3     50.00   PATH
RF[29]                    16.7     89.3     38.9     39.3     50.00   PATH
RF[2]                     13.7     89.3     38.9     39.3     50.00   PATH
RF[30]                    89.3     89.3     39.3     39.3     50.00   PATH
RF[31]                    89.3     89.3     39.3     39.3     50.00   PATH
RF[3]                     13.7     89.3     38.9     39.3     50.00   PATH
RF[4]                     13.5     89.3     38.9     39.3     50.00   PATH
RF[5]                     13.5     89.3     38.9     39.3     50.00   PATH
RF[6]                     13.4     89.3     38.9     39.3     50.00   PATH
```

RF[7]	13.4	89.3	38.9	39.3	50.00	PATH
RF[8]	13.9	89.3	38.9	39.3	50.00	PATH
RF[9]	13.4	89.3	38.9	39.3	50.00	PATH
RF_adr[0]	12.7	44.9	14.0	15.3	50.00	PATH
RF_adr[10]	12.9	45.0	14.2	15.4	50.00	PATH
RF_adr[11]	12.9	45.0	14.2	15.4	50.00	PATH
RF_adr[12]	12.9	45.0	14.2	15.4	50.00	PATH
RF_adr[13]	12.9	45.0	14.2	15.4	50.00	PATH
RF_adr[14]	12.9	45.0	14.2	15.4	50.00	PATH
RF_adr[15]	12.9	45.0	14.2	15.4	50.00	PATH
RF_adr[16]	12.9	45.0	14.2	15.4	50.00	PATH
RF_adr[17]	12.9	45.1	14.2	15.5	50.00	PATH
RF_adr[18]	12.9	45.0	14.2	15.5	50.00	PATH
RF_adr[19]	12.9	45.1	14.3	15.5	50.00	PATH
RF_adr[1]	12.8	44.9	14.1	15.3	50.00	PATH
RF_adr[20]	13.0	45.1	14.3	15.5	50.00	PATH
RF_adr[21]	13.0	45.1	14.3	15.5	50.00	PATH
RF_adr[22]	13.0	45.1	14.3	15.5	50.00	PATH
RF_adr[23]	13.1	45.2	14.4	15.6	50.00	PATH
RF_adr[24]	13.1	45.2	14.4	15.6	50.00	PATH
RF_adr[25]	13.1	45.2	14.4	15.6	50.00	PATH
RF_adr[2]	12.8	44.9	14.1	15.3	50.00	PATH
RF_adr[3]	12.8	45.0	14.1	15.4	50.00	PATH
RF_adr[4]	12.8	45.0	14.1	15.4	50.00	PATH
RF_adr[5]	12.8	45.0	14.1	15.4	50.00	PATH
RF_adr[6]	12.8	45.0	14.2	15.4	50.00	PATH
RF_adr[7]	12.9	45.0	14.2	15.4	50.00	PATH
RF_adr[8]	12.9	45.0	14.2	15.4	50.00	PATH
RF_adr[9]	12.9	45.0	14.2	15.4	50.00	PATH
RF_adr_mode[0]	10.1	10.6	9.9	23.5	50.00	PATH
RF_adr_mode[1]	10.1	10.6	9.9	23.5	50.00	PATH
RF_adr_mode[2]	10.1	10.6	9.9	23.5	50.00	PATH
RF_adr_mode[3]	10.1	10.6	9.8	23.5	50.00	PATH
RF_off[0]	11.0	11.5	9.9	24.4	50.00	PATH
RF_off[10]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[11]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[12]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[13]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[14]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[15]	11.0	11.5	10.3	24.4	50.00	PATH
RF_off[16]	11.0	11.5	10.3	24.4	50.00	PATH
RF_off[17]	11.0	11.5	10.0	24.4	50.00	PATH
RF_off[18]	11.0	11.5	10.1	24.4	50.00	PATH
RF_off[19]	11.0	11.5	10.1	24.4	50.00	PATH
RF_off[1]	11.0	11.5	9.9	24.4	50.00	PATH
RF_off[20]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[21]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[22]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[23]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[24]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[25]	11.0	11.5	10.2	24.4	50.00	PATH
RF_off[2]	11.0	11.5	9.9	24.4	50.00	PATH
RF_off[3]	11.0	11.5	9.9	24.4	50.00	PATH
RF_off[4]	11.0	11.5	10.0	24.4	50.00	PATH
RF_off[5]	11.0	11.5	10.0	24.4	50.00	PATH
RF_off[6]	11.0	11.5	10.0	24.4	50.00	PATH
RF_off[7]	11.0	11.5	10.1	24.4	50.00	PATH
RF_off[8]	11.0	11.5	10.1	24.4	50.00	PATH
RF_off[9]	11.0	11.5	10.1	24.4	50.00	PATH
R_eq_f_1	13.4	57.6	---	---	50.00	PATH
R_eq_f_2	13.2	57.6	---	---	50.00	PATH
SF_adr[0]	12.8	45.2	14.1	15.8	50.00	PATH

```
SF_adr[10]              13.0    45.3    14.3    16.0    50.00   PATH
SF_adr[11]              13.0    45.3    14.3    16.0    50.00   PATH
SF_adr[12]              13.0    45.3    14.3    16.0    50.00   PATH
SF_adr[13]              13.0    45.3    14.3    16.0    50.00   PATH
SF_adr[14]              13.0    45.4    14.3    16.0    50.00   PATH
SF_adr[15]              13.1    45.4    14.4    16.1    50.00   PATH
SF_adr[16]              13.1    45.4    14.4    16.1    50.00   PATH
SF_adr[17]              13.1    45.4    14.4    16.1    50.00   PATH
SF_adr[18]              13.2    45.4    14.5    16.1    50.00   PATH
SF_adr[19]              13.2    45.5    14.5    16.1    50.00   PATH
SF_adr[1]               12.7    45.2    14.0    15.8    50.00   PATH
SF_adr[20]              13.2    45.5    14.5    16.2    50.00   PATH
SF_adr[21]              13.2    45.5    14.5    16.2    50.00   PATH
SF_adr[22]              13.2    45.5    14.5    16.2    50.00   PATH
SF_adr[23]              13.3    45.5    14.6    16.2    50.00   PATH
SF_adr[24]              13.3    45.6    14.6    16.2    50.00   PATH
SF_adr[25]              13.3    45.6    14.6    16.2    50.00   PATH
SF_adr[2]               12.7    45.2    14.1    15.8    50.00   PATH
SF_adr[3]               12.8    45.2    14.1    15.8    50.00   PATH
SF_adr[4]               12.8    45.2    14.1    15.9    50.00   PATH
SF_adr[5]               12.8    45.2    14.1    15.9    50.00   PATH
SF_adr[6]               12.8    45.2    14.1    15.9    50.00   PATH
SF_adr[7]               12.9    45.3    14.2    15.9    50.00   PATH
SF_adr[8]               12.9    45.3    14.2    15.9    50.00   PATH
SF_adr[9]               12.9    45.3    14.2    16.0    50.00   PATH
S_adr_mode[0]           10.3    10.7    11.7    23.6    50.00   PATH
S_adr_mode[1]           10.3    10.7    11.7    23.6    50.00   PATH
S_adr_mode[2]           10.3    10.7    11.7    23.6    50.00   PATH
S_adr_mode[3]           10.3    10.7    11.7    23.6    50.00   PATH
S_eq_f_1                13.0    57.3     ---     ---    50.00   PATH
S_eq_f_2                12.9    57.2     ---     ---    50.00   PATH
S_off[0]                11.1    11.6    10.1    24.5    50.00   PATH
S_off[10]               11.1    11.6    10.6    24.5    50.00   PATH
S_off[11]               11.1    11.6    10.7    24.5    50.00   PATH
S_off[12]               11.1    11.6    10.7    24.5    50.00   PATH
S_off[13]               11.1    11.6    10.7    24.5    50.00   PATH
S_off[14]               11.1    11.6    10.8    24.5    50.00   PATH
S_off[15]               11.1    11.6    10.9    24.5    50.00   PATH
S_off[16]               11.1    11.6    11.0    24.5    50.00   PATH
S_off[17]               11.1    11.6    10.9    24.5    50.00   PATH
S_off[18]               11.1    11.6    11.0    24.5    50.00   PATH
S_off[19]               11.1    11.6    11.0    24.5    50.00   PATH
S_off[1]                11.1    11.6    10.1    24.5    50.00   PATH
S_off[20]               11.1    11.6    11.0    24.5    50.00   PATH
S_off[21]               11.1    11.6    11.1    24.5    50.00   PATH
S_off[22]               11.1    11.6    11.2    24.5    50.00   PATH
S_off[23]               11.1    11.6    11.4    24.5    50.00   PATH
S_off[24]               11.1    11.6    11.3    24.5    50.00   PATH
S_off[25]               11.1    11.6    11.3    24.5    50.00   PATH
S_off[2]                11.1    11.6    10.2    24.5    50.00   PATH
S_off[3]                11.1    11.6    10.2    24.5    50.00   PATH
S_off[4]                11.1    11.6    10.3    24.5    50.00   PATH
S_off[5]                11.1    11.6    10.3    24.5    50.00   PATH
S_off[6]                11.1    11.6    10.4    24.5    50.00   PATH
S_off[7]                11.1    11.6    10.4    24.5    50.00   PATH
S_off[8]                11.1    11.6    10.4    24.5    50.00   PATH
S_off[9]                11.1    11.6    10.7    24.5    50.00   PATH
 ****************************************************************************
              Genesil Version v8.0.2 -- Thu Jan 24 14:16:44 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
****************************************************************************
PATH DELAY MODE
```

```
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: TYPICAL
  Junction Temperature:75 deg C         Voltage:5.00v
  External Clock: Clk
 Included setup files:
  #0  clock_output            (Clock time, output delay)
--------------------------------------------------------------------------------
                                PATH DELAY (ns)
Source Object     Connector           (Ph1) Min      Max
   Dest. Object       Connector       (Ph2)    Min       Max

 _______________ _________________
 clock_pad______ PHASE_A_________         5.4     16.7

    _____________ _________________
    odc_rf_mod/odc_> rf_adr[0]_____         8.7      8.8  PATH

 _______________ _________________
 clock_pad______ PHASE_A_________         2.5      3.9

    _____________ _________________
    odc_rf_mod/odc_> ods_sel_______         4.0      4.0  PATH

 _______________ _________________
 odc_rf_mod/odc_ ods_sel_________         8.6     11.3

    _____________ _________________
    rf_adr_pad[0]___ RF_adr________         8.6     11.3  PATH

 _______________ _________________
 clock_pad______ PHASE_A_________         0.0      0.0

    _____________ _________________
    odc_rf_mod/odc_> PHASE_A_______         0.0      0.0  PATH

 _______________ _________________
 odc_rf_mod/odc_ PHASE_A_________         9.6     11.3

    _____________ _________________
    rf_adr_pad[0]___ RF_adr________         ---      ---  PATH

 _______________ _________________
 odc_rf_mod/odc_ ods_sel_________         9.0     11.5

    _____________ _________________
    rf_adr_pad[25]__ RF_adr________         9.0     11.5  PATH

 _______________ _________________
 odc_rf_mod/odc_ ods_sel_________         8.6     10.8

    _____________ _________________
    s_adr_pad[0]____ SF_adr________         8.6     10.8  PATH

 _______________ _________________
 odc_rf_mod/odc_ ods_sel_________         9.2     11.2

    _____________ _________________
    s_adr_pad[25]___ SF_adr________         9.2     11.2  PATH
 _______________ _________________
>_______________ _________________

    _____________ _________________
    _____________ _________________
 ********************************************************************************
             Genesil Version v8.0.2 -- Thu Jan 24 14:20:52 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
********************************************************************************
SETUP AND HOLD MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: TYPICAL
  Junction Temperature:75 deg C         Voltage:5.00v
  External Clock: Clk
 Included setup files:
  #0  setup_hold              (Setup/Hold time, Violations)
--------------------------------------------------------------------------------
                        INPUT SETUP AND HOLD TIMES (ns)
Input                     Setup Time            Hold Time
                         Ph1(f)   Ph2(f)      Ph1(f)   Ph2(f)
Booting                    ---      12.2        ---      -5.0       PATH
```

DAG_R_en	---	---	---	---	PATH
Flush	---	22.1	---	-0.7	PATH
Freeze	---	21.7	---	-2.6	PATH
Guard	---	7.3	---	-3.9	PATH
Ids_eq_ods_1	---	7.2	---	-5.6	PATH
Ids_eq_ods_2	---	7.0	---	-5.4	PATH
Ids_freeze	---	2.6	---	-0.9	PATH
Inst_en	---	3.3	---	-1.5	PATH
Inst_rd	---	7.5	---	-3.4	PATH
Kernel_mode	---	30.5	---	-2.7	PATH
N_reset	---	23.8	---	-1.6	PATH
Ods_freeze	2.6	---	-1.0	---	PATH
Pc[0]	---	11.9	---	-1.8	PATH
Pc[1]	---	12.2	---	-1.9	PATH
Pc[2]	---	12.9	---	-1.8	PATH
Pc[3]	---	12.6	---	-3.2	PATH
RF[0]	2.4	3.4	-1.7	-2.5	PATH
RF[10]	1.8	2.8	-1.1	-1.9	PATH
RF[11]	1.8	2.8	-1.0	-1.8	PATH
RF[12]	1.7	2.7	-0.9	-1.7	PATH
RF[13]	1.7	2.7	-0.9	-1.7	PATH
RF[14]	1.7	2.7	-0.9	-1.7	PATH
RF[15]	1.7	2.7	-0.9	-1.7	PATH
RF[16]	1.6	2.6	-0.9	-1.7	PATH
RF[17]	1.6	2.6	-0.8	-1.6	PATH
RF[18]	1.6	2.6	-0.8	-1.6	PATH
RF[19]	2.0	3.0	-1.2	-2.0	PATH
RF[1]	2.0	3.0	-1.3	-2.1	PATH
RF[20]	1.9	2.9	-1.2	-2.0	PATH
RF[21]	1.7	2.7	-1.0	-1.8	PATH
RF[22]	1.7	2.7	-0.9	-1.7	PATH
RF[23]	1.9	2.9	-1.1	-1.9	PATH
RF[24]	1.7	2.7	-0.9	-1.7	PATH
RF[25]	1.6	2.6	-0.9	-1.7	PATH
RF[26]	1.6	2.6	-0.8	-1.6	PATH
RF[27]	1.6	2.6	-0.8	-1.6	PATH
RF[28]	1.4	2.4	-0.6	-1.4	PATH
RF[29]	0.8	1.8	0.1	-0.7	PATH
RF[2]	2.0	3.0	-1.2	-2.0	PATH
RF[30]	---	---	---	---	PATH
RF[31]	---	---	---	---	PATH
RF[3]	2.0	3.0	-1.3	-2.1	PATH
RF[4]	1.9	2.9	-1.2	-2.0	PATH
RF[5]	1.9	2.9	-1.2	-2.0	PATH
RF[6]	1.9	2.9	-1.1	-1.9	PATH
RF[7]	1.9	2.9	-1.1	-1.9	PATH
RF[8]	1.9	2.9	-1.1	-1.9	PATH
RF[9]	1.8	2.8	-1.1	-1.9	PATH
RF_adr_mode[0]	6.1	6.4	-2.8	-3.6	PATH
RF_adr_mode[1]	6.2	6.5	-2.8	-3.5	PATH
RF_adr_mode[2]	4.9	5.2	-2.8	-3.6	PATH
RF_adr_mode[3]	4.6	4.8	-2.2	-3.2	PATH
RF_off[0]	4.5	5.4	-4.0	-3.4	PATH
RF_off[10]	4.4	5.3	-3.9	-3.3	PATH
RF_off[11]	4.3	5.2	-3.8	-3.3	PATH
RF_off[12]	4.3	5.2	-3.8	-3.2	PATH
RF_off[13]	4.3	5.2	-3.8	-3.2	PATH
RF_off[14]	4.3	5.2	-3.8	-3.3	PATH
RF_off[15]	4.3	5.2	-3.8	-3.3	PATH
RF_off[16]	4.3	5.2	-3.8	-3.3	PATH
RF_off[17]	4.4	5.3	-3.9	-3.4	PATH
RF_off[18]	4.4	5.3	-3.9	-3.3	PATH

```
RF_off[19]                4.5      5.5       -4.1      -3.5      PATH
RF_off[1]                 4.5      5.4       -4.0      -3.4      PATH
RF_off[20]                4.6      5.5       -4.1      -3.5      PATH
RF_off[21]                4.6      5.5       -4.1      -3.5      PATH
RF_off[22]                4.6      5.5       -4.1      -3.6      PATH
RF_off[23]                4.6      5.6       -4.1      -3.6      PATH
RF_off[24]                4.7      5.6       -4.2      -3.6      PATH
RF_off[25]                4.7      5.6       -4.2      -3.7      PATH
RF_off[2]                 4.7      5.6       -4.2      -3.6      PATH
RF_off[3]                 4.7      5.6       -4.2      -3.6      PATH
RF_off[4]                 4.6      5.5       -4.1      -3.6      PATH
RF_off[5]                 4.6      5.5       -4.1      -3.6      PATH
RF_off[6]                 4.5      5.5       -4.1      -3.5      PATH
RF_off[7]                 4.5      5.4       -4.0      -3.5      PATH
RF_off[8]                 4.2      5.2       -3.8      -3.2      PATH
RF_off[9]                 4.4      5.3       -3.9      -3.4      PATH
S_adr_mode[0]             ---      6.6        ---      -3.1      PATH
S_adr_mode[1]             ---      6.6        ---      -3.0      PATH
S_adr_mode[2]             ---      5.0        ---      -3.0      PATH
S_adr_mode[3]             ---      5.0        ---      -3.1      PATH
S_off[0]                  ---      4.0        ---      -2.6      PATH
S_off[10]                 ---      4.2        ---      -2.8      PATH
S_off[11]                 ---      4.2        ---      -2.8      PATH
S_off[12]                 ---      4.2        ---      -2.8      PATH
S_off[13]                 ---      4.3        ---      -2.9      PATH
S_off[14]                 ---      4.3        ---      -2.9      PATH
S_off[15]                 ---      4.4        ---      -3.0      PATH
S_off[16]                 ---      4.4        ---      -3.0      PATH
S_off[17]                 ---      4.5        ---      -3.1      PATH
S_off[18]                 ---      4.5        ---      -3.1      PATH
S_off[19]                 ---      4.5        ---      -3.2      PATH
S_off[1]                  ---      4.0        ---      -2.6      PATH
S_off[20]                 ---      4.6        ---      -3.2      PATH
S_off[21]                 ---      4.6        ---      -3.2      PATH
S_off[22]                 ---      4.6        ---      -3.3      PATH
S_off[23]                 ---      4.7        ---      -3.4      PATH
S_off[24]                 ---      4.8        ---      -3.4      PATH
S_off[25]                 ---      4.7        ---      -3.3      PATH
S_off[2]                  ---      4.0        ---      -2.6      PATH
S_off[3]                  ---      4.0        ---      -2.6      PATH
S_off[4]                  ---      4.0        ---      -2.6      PATH
S_off[5]                  ---      4.0        ---      -2.6      PATH
S_off[6]                  ---      4.0        ---      -2.6      PATH
S_off[7]                  ---      4.0        ---      -2.6      PATH
S_off[8]                  ---      4.0        ---      -2.6      PATH
S_off[9]                  ---      4.1        ---      -2.7      PATH
Valid_intr                ---     20.5        ---      -1.9      PATH
 ********************************************************************************
             Genesil Version v8.0.2 -- Thu Jan 24 14:21:57 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
********************************************************************************
VIOLATION MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: TYPICAL
  Junction Temperature:75 deg C         Voltage:5.00v
  External Clock: Clk
 Included setup files:
  #0  setup_hold              (Setup/Hold time, Violations)
--------------------------------------------------------------------------------
                                NO VIOLATIONS
  Hold time check margin: 2.0ns
```

13.2. GUARANTEED, Max T, Min V

```
*******************************************************************************
              Genesil Version v8.0.2 -- Fri Jan 18 12:11:37 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
*******************************************************************************
CLOCK REPORT MODE
-------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: GUARANTEED
  Junction Temperature:112 deg C        Voltage:4.50v
  External Clock: Clk
 Included setup files:
  #0  set_hot                (Setup/Hold time, Violations -- Ma>
-------------------------------------------------------------------------------
                            CLOCK TIMES (minimum)
Phase 1 High:    51.1   ns             Phase 2 High:    64.6   ns
              ----------                            ----------
Cycle (from Ph1):   113.1   ns         Cycle (from Ph2):   125.2   ns
                 ----------                            ----------
Minimum Cycle Time:   125.2   ns       Symmetric Cycle Time:    129.2   ns
                    ----------                           ----------
-------------------------------------------------------------------------------
                            CLOCK WORST CASE PATHS
Minimum Phase 1 high time is    51.1   ns set by:
                            ----------
  ** Clock delay: 4.4ns (55.5-51.1)
   Node                              Cumulative Delay      Transition
   <dr_gen/critical_rl/(internal)      55.5                  rise
   f_adr_gen/critical_rl/mnz           53.0                  fall
   <en/critical_rl/f_boot_mode[0]      51.0                  rise
   <n/critical_rl/f_boot_mode[0]'      50.0                  rise
   <adr_gen/critical_rl/n_mode[0]      49.2                  fall
   <en/critical_rl/rf_adr_mode[0]      48.7                  rise
   rf_mode_pad[0]/rf_adr_mode          48.3                  rise
   rf_mode_pad[0]/rf_adr_mode'         43.6                  rise
   RF_adr_mode[0]                      40.0                  rise


Minimum Phase 2 high time is    64.6   ns set by:
                            ----------
  ** Clock delay: 4.1ns (68.7-64.6)
   Node                              Cumulative Delay      Transition
   <ptr_mod/adr_ptr_dp/(internal)      68.7                  rise
   <_mod/adr_ptr_dp/INTER4_ST1[4]      63.5                  fall
   <tr_mod/adr_ptr_dp/adr_ptr_sel      58.0                  fall
   <_mod/adr_ptr_ctrl/adr_ptr_sel      58.0                  fall
   <mod/adr_ptr_ctrl/adr_ptr_sel'      56.0                  fall
   <tr_mod/adr_ptr_ctrl/decrement      54.2                  fall
   <r_mod/adr_ptr_ctrl/decrement'      51.2                  fall
   <_ptr_mod/adr_ptr_ctrl/dec_mux      49.3                  fall
   <ptr_mod/adr_ptr_ctrl/dec_mux'      49.2                  fall
   <r_mod/adr_ptr_ctrl/decr_ap_in      47.2                  fall
   <_mod/adr_ptr_ctrl/decr_ap_in'      46.6                  fall
   <_mod/adr_ptr_ctrl/n_res_fl_fr      44.7                  fall
   <mod/adr_ptr_ctrl/n_res_fl_fr'      44.6                  fall
   <r_ptr_mod/adr_ptr_ctrl/freeze      42.5                  rise
   <mod/adr_ptr_ctrl/n_freeze_buf      41.5                  fall
   <od/adr_ptr_ctrl/n_freeze_buf'      41.4                  fall
   <ptr_mod/adr_ptr_ctrl/n_freeze      39.8                  fall
   freeze_pad/n_freeze                 35.3                  fall
   freeze_pad/n_freeze'                29.3                  fall
   Freeze                              26.7                  rise
```

```
Minimum cycle time (from Ph1) is  113.1    ns set by:
                                  ----------
  ** Clock delay: 7.0ns (120.1-113.1)
   Node                              Cumulative Delay      Transition
   <toZ5fnowZ2eresetZ5fsigZ5b0Z5d      120.1                  fall
   <gen/super_ctrl/GB.LP.NNZ5fN49      119.7                  rise
   <.NNflagsZ2ftoZ5fnowZ2esetZ5fy      118.6                  fall
   *<en/super_ctrl/GB.LP.NNZ5fN45      115.7                  fall
   <_gen/super_ctrl/GB.LP.NNZ5fN2      115.2                  rise
   <dr_gen/super_ctrl/n_adr_under      114.4                  fall
   f_adr_gen/super_dp/n_adr_under      114.3                  fall
   <adr_gen/super_dp/n_adr_under'      112.8                  fall
   f_adr_gen/super_dp/adr[2]            81.9                  fall
   f_adr_gen/super_dp/adr[2]'           81.0                  fall
   <r_gen/super_dp/ea_tpap_OUT[2]       76.8                  fall
   <adr_gen/super_dp/no_tp_ST2[1]       69.4                  fall
   <_gen/super_dp/eff_adrl_OUT[1]       67.8                  fall
   <_gen/super_dp/eff_adrl_IN1[0]       60.7                  fall
   <dr_gen/super_dp/mode_not_zero       56.4                  fall
   <gen/critical_rl/mode_not_zero       56.4                  fall
   <en/critical_rl/mode_not_zero'       55.9                  fall
   f_adr_gen/critical_rl/mnz            53.0                  fall
   <en/critical_rl/f_boot_mode[0]       51.0                  rise
   <n/critical_rl/f_boot_mode[0]'       50.0                  rise
   <adr_gen/critical_rl/n_mode[0]       49.2                  fall
   <en/critical_rl/rf_adr_mode[0]       48.7                  rise
   rf_mode_pad[0]/rf_adr_mode           48.3                  rise
   rf_mode_pad[0]/rf_adr_mode'          43.6                  rise
   RF_adr_mode[0]                       40.0                  rise

Minimum cycle time (from Ph2) is  125.2    ns set by:
                                  ----------
  ** Clock delay: 6.5ns (131.7-125.2)
   Node                              Cumulative Delay      Transition
   error_mod/error_ff/s_eq_f_2         131.7                  rise
   odc_rf_mod/odc_mux/odc_out[1]       131.7                  rise
   odc_rf_mod/odc_mux/odc_out[1]'      130.3                  rise
   <_rf_mod/odc_mux/INTER0_ST1[1]      127.0                  rise
   odc_rf_mod/odc_mux/odc_in[1]        125.1                  rise
   odc_rf_mod/odc_ctrl/s2              125.1                  rise
   odc_rf_mod/odc_ctrl/s2'             124.0                  rise
   <rf_mod/odc_ctrl/GB.LP.NNZ5fN2      123.6                  fall
   odc_rf_mod/odc_ctrl/s2_int          123.1                  rise
   odc_rf_mod/odc_rf_dp/s_eq_f_2       123.1                  rise
   odc_rf_mod/odc_rf_dp/s_eq_f_2'      122.4                  rise
   odc_rf_mod/odc_rf_dp/s_adr[25]      117.8                  rise
   s_adr_gen/super_dp/adr[25]          117.1                  rise
   s_adr_gen/super_dp/adr[25]'         116.4                  rise
   <_gen/super_dp/ea_tpap_OUT[25]      112.5                  rise
   <r_gen/super_dp/bring_b_ST1[0]       79.9                  fall
   s_adr_gen/super_dp/adr_ptr[0]        77.6                  fall
   <ptr_mod/adr_ptr_dp/adr_ptr[0]       77.0                  fall
   <tr_mod/adr_ptr_dp/adr_ptr[0]'       73.9                  fall
   <mod/adr_ptr_dp/INTER5_VAL1[0]       71.8                  fall
   *<tr_mod/adr_ptr_dp/(internal)       69.1                  fall
   <_mod/adr_ptr_dp/INTER4_ST1[0]       63.5                  fall
   <tr_mod/adr_ptr_dp/adr_ptr_sel       58.0                  fall
   <_mod/adr_ptr_ctrl/adr_ptr_sel       58.0                  fall
   <mod/adr_ptr_ctrl/adr_ptr_sel'       56.0                  fall
   <tr_mod/adr_ptr_ctrl/decrement       54.2                  fall
   <r_mod/adr_ptr_ctrl/decrement'       51.2                  fall
   <_ptr_mod/adr_ptr_ctrl/dec_mux       49.3                  fall
```

```
   <ptr_mod/adr_ptr_ctrl/dec_mux'      49.2              fall
   <r_mod/adr_ptr_ctrl/decr_ap_in      47.2              fall
   <_mod/adr_ptr_ctrl/decr_ap_in'      46.6              fall
   <_mod/adr_ptr_ctrl/n_res_fl_fr      44.7              fall
   <mod/adr_ptr_ctrl/n_res_fl_fr'      44.6              fall
   <r_ptr_mod/adr_ptr_ctrl/freeze      42.5              rise
   <mod/adr_ptr_ctrl/n_freeze_buf      41.5              fall
   <od/adr_ptr_ctrl/n_freeze_buf'      41.4              fall
   <ptr_mod/adr_ptr_ctrl/n_freeze      39.8              fall
   freeze_pad/n_freeze                 35.3              fall
cd   freeze_pad/n_freeze'                29.3               fall
   Freeze                              26.7              rise
--------------------------------------------------------------------------------
 ********************************************************************************
            Genesil Version v8.0.2 -- Fri Jan 18 12:11:40 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                  Timing Analyzer
********************************************************************************
OUTPUT DELAY MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: GUARANTEED
  Junction Temperature:112 deg C        Voltage:4.50v
  External Clock: Clk
 Included setup files:
  #0  set_hot                (Setup/Hold time, Violations -- Ma>
--------------------------------------------------------------------------------
                              OUTPUT DELAYS (ns)
Output                    Ph1(r) Delay      Ph2(r) Delay      Loading(pf)
                          Min      Max      Min      Max
DAG_Error                 30.7     34.9     ---      ---      50.00   PATH
RF[0]                     26.6     77.9     45.5     45.7     50.00   PATH
RF[10]                    25.3     77.7     45.3     45.5     50.00   PATH
RF[11]                    25.2     77.9     45.5     45.7     50.00   PATH
RF[12]                    25.3     77.9     45.5     45.7     50.00   PATH
RF[13]                    28.1     78.0     45.6     45.8     50.00   PATH
RF[14]                    28.1     78.0     45.6     45.8     50.00   PATH
RF[15]                    28.1     78.0     45.6     45.8     50.00   PATH
RF[16]                    28.1     78.0     45.6     45.8     50.00   PATH
RF[17]                    29.0     78.1     45.7     45.9     50.00   PATH
RF[18]                    30.0     78.1     45.7     45.9     50.00   PATH
RF[19]                    29.9     78.1     45.7     45.9     50.00   PATH
RF[1]                     26.3     77.8     45.4     45.6     50.00   PATH
RF[20]                    30.3     78.2     45.8     46.0     50.00   PATH
RF[21]                    30.2     78.2     45.8     46.0     50.00   PATH
RF[22]                    28.3     78.2     45.8     46.0     50.00   PATH
RF[23]                    30.1     78.2     45.8     46.0     50.00   PATH
RF[24]                    30.0     78.2     45.8     46.0     50.00   PATH
RF[25]                    29.8     78.2     45.8     46.0     50.00   PATH
RF[26]                    31.6     78.2     45.8     46.0     50.00   PATH
RF[27]                    31.4     78.2     45.8     46.0     50.00   PATH
RF[28]                    31.3     78.2     45.8     46.0     50.00   PATH
RF[29]                    31.2     78.2     45.9     46.1     50.00   PATH
RF[2]                     26.2     77.8     45.4     45.6     50.00   PATH
RF[30]                    78.3     78.3     46.1     46.1     50.00   PATH
RF[31]                    78.3     78.3     46.1     46.1     50.00   PATH
RF[3]                     26.1     77.8     45.4     45.6     50.00   PATH
RF[4]                     25.8     77.8     45.4     45.6     50.00   PATH
RF[5]                     25.5     77.8     45.4     45.6     50.00   PATH
RF[6]                     25.4     77.8     45.4     45.6     50.00   PATH
RF[7]                     25.4     77.8     45.4     45.6     50.00   PATH
RF[8]                     26.3     77.8     45.4     45.6     50.00   PATH
RF[9]                     25.3     77.7     45.3     45.5     50.00   PATH
RF_adr[0]                 23.5     60.4     25.9     27.4     50.00   PATH
```

RF_adr[10]	23.9	60.8	26.3	27.7	50.00	PATH
RF_adr[11]	23.9	61.5	26.3	27.8	50.00	PATH
RF_adr[12]	23.9	62.6	26.3	27.8	50.00	PATH
RF_adr[13]	23.9	63.6	26.3	27.8	50.00	PATH
RF_adr[14]	23.9	64.8	26.3	27.8	50.00	PATH
RF_adr[15]	24.0	65.8	26.4	27.8	50.00	PATH
RF_adr[16]	24.0	67.0	26.4	27.9	50.00	PATH
RF_adr[17]	24.1	68.1	26.5	27.9	50.00	PATH
RF_adr[18]	24.0	69.2	26.4	27.9	50.00	PATH
RF_adr[19]	24.1	70.2	26.5	28.0	50.00	PATH
RF_adr[1]	23.5	60.5	25.9	27.5	50.00	PATH
RF_adr[20]	24.3	71.5	26.7	28.1	50.00	PATH
RF_adr[21]	24.4	72.6	26.8	28.2	50.00	PATH
RF_adr[22]	24.5	73.8	26.9	28.2	50.00	PATH
RF_adr[23]	24.6	75.0	27.0	28.4	50.00	PATH
RF_adr[24]	24.7	76.2	27.1	28.4	50.00	PATH
RF_adr[25]	24.7	77.1	27.1	28.4	50.00	PATH
RF_adr[2]	23.5	60.5	25.9	27.4	50.00	PATH
RF_adr[3]	23.7	60.6	26.1	27.6	50.00	PATH
RF_adr[4]	23.7	60.6	26.1	27.6	50.00	PATH
RF_adr[5]	23.8	60.6	26.2	27.6	50.00	PATH
RF_adr[6]	23.8	60.7	26.2	27.7	50.00	PATH
RF_adr[7]	23.8	60.7	26.2	27.7	50.00	PATH
RF_adr[8]	23.9	60.8	26.3	27.8	50.00	PATH
RF_adr[9]	23.8	60.7	26.2	27.7	50.00	PATH
RF_adr_mode[0]	18.8	19.0	18.3	31.9	50.00	PATH
RF_adr_mode[1]	18.8	19.0	18.2	31.9	50.00	PATH
RF_adr_mode[2]	18.8	19.0	18.2	31.9	50.00	PATH
RF_adr_mode[3]	18.8	19.0	18.0	31.9	50.00	PATH
RF_off[0]	21.8	22.0	18.3	34.9	50.00	PATH
RF_off[10]	21.7	21.9	18.9	34.8	50.00	PATH
RF_off[11]	21.7	21.9	18.9	34.8	50.00	PATH
RF_off[12]	21.7	21.9	18.9	34.8	50.00	PATH
RF_off[13]	21.7	21.9	19.0	34.8	50.00	PATH
RF_off[14]	21.7	21.8	19.0	34.7	50.00	PATH
RF_off[15]	21.6	21.8	19.1	34.7	50.00	PATH
RF_off[16]	21.6	21.8	19.1	34.7	50.00	PATH
RF_off[17]	21.5	21.7	18.5	34.6	50.00	PATH
RF_off[18]	21.5	21.7	18.6	34.6	50.00	PATH
RF_off[19]	21.5	21.7	18.7	34.6	50.00	PATH
RF_off[1]	21.8	22.0	18.2	34.9	50.00	PATH
RF_off[20]	21.5	21.7	19.0	34.6	50.00	PATH
RF_off[21]	21.5	21.7	18.8	34.6	50.00	PATH
RF_off[22]	21.5	21.7	18.9	34.6	50.00	PATH
RF_off[23]	21.5	21.7	18.8	34.6	50.00	PATH
RF_off[24]	21.5	21.7	18.9	34.6	50.00	PATH
RF_off[25]	21.5	21.7	19.0	34.6	50.00	PATH
RF_off[2]	21.8	22.0	18.1	34.9	50.00	PATH
RF_off[3]	21.8	22.0	18.2	34.9	50.00	PATH
RF_off[4]	21.8	22.0	18.5	34.9	50.00	PATH
RF_off[5]	21.8	22.0	18.5	34.9	50.00	PATH
RF_off[6]	21.8	22.0	18.5	34.9	50.00	PATH
RF_off[7]	21.8	22.0	18.6	34.9	50.00	PATH
RF_off[8]	21.8	22.0	18.7	34.9	50.00	PATH
RF_off[9]	21.7	21.9	18.6	34.8	50.00	PATH
R_eq_f_1	22.9	82.2	---	---	50.00	PATH
R_eq_f_2	22.6	82.5	---	---	50.00	PATH
SF_adr[0]	23.4	62.1	25.8	28.3	50.00	PATH
SF_adr[10]	24.0	62.5	26.4	28.8	50.00	PATH
SF_adr[11]	24.1	63.2	26.5	28.9	50.00	PATH
SF_adr[12]	24.2	64.4	26.6	28.9	50.00	PATH
SF_adr[13]	24.3	65.4	26.7	29.0	50.00	PATH

```
SF_adr[14]                24.4     66.7     26.8     29.1      50.00   PATH
SF_adr[15]                24.6     67.8     27.0     29.2      50.00   PATH
SF_adr[16]                24.6     69.0     27.0     29.2      50.00   PATH
SF_adr[17]                24.7     70.1     27.1     29.4      50.00   PATH
SF_adr[18]                24.8     71.3     27.2     29.5      50.00   PATH
SF_adr[19]                24.9     72.4     27.3     29.5      50.00   PATH
SF_adr[1]                 23.4     62.0     25.8     28.2      50.00   PATH
SF_adr[20]                25.0     73.7     27.4     29.6      50.00   PATH
SF_adr[21]                25.0     74.7     27.4     29.6      50.00   PATH
SF_adr[22]                25.1     76.0     27.5     29.7      50.00   PATH
SF_adr[23]                25.2     77.1     27.6     29.8      50.00   PATH
SF_adr[24]                25.3     78.3     27.7     29.8      50.00   PATH
SF_adr[25]                25.5     79.5     27.9     30.0      50.00   PATH
SF_adr[2]                 23.4     62.0     25.8     28.2      50.00   PATH
SF_adr[3]                 23.5     62.1     25.9     28.3      50.00   PATH
SF_adr[4]                 23.5     62.1     25.9     28.4      50.00   PATH
SF_adr[5]                 23.6     62.2     26.0     28.4      50.00   PATH
SF_adr[6]                 23.7     62.2     26.1     28.5      50.00   PATH
SF_adr[7]                 23.8     62.3     26.2     28.5      50.00   PATH
SF_adr[8]                 23.9     62.4     26.3     28.7      50.00   PATH
SF_adr[9]                 24.0     62.5     26.4     28.8      50.00   PATH
S_adr_mode[0]             19.3     19.5     23.9     32.4      50.00   PATH
S_adr_mode[1]             19.3     19.5     23.8     32.4      50.00   PATH
S_adr_mode[2]             19.3     19.5     23.6     32.4      50.00   PATH
S_adr_mode[3]             19.3     19.5     23.5     32.4      50.00   PATH
S_eq_f_1                  23.4     83.4      ---      ---      50.00   PATH
S_eq_f_2                  23.2     83.4      ---      ---      50.00   PATH
S_off[0]                  21.7     21.9     18.7     34.8      50.00   PATH
S_off[10]                 22.1     22.3     20.1     35.2      50.00   PATH
S_off[11]                 22.1     22.3     20.2     35.2      50.00   PATH
S_off[12]                 22.2     22.4     20.2     35.3      50.00   PATH
S_off[13]                 22.2     22.4     20.3     35.3      50.00   PATH
S_off[14]                 22.2     22.4     20.4     35.3      50.00   PATH
S_off[15]                 22.2     22.4     20.7     35.3      50.00   PATH
S_off[16]                 22.2     22.4     20.8     35.3      50.00   PATH
S_off[17]                 22.3     22.5     20.8     35.4      50.00   PATH
S_off[18]                 22.3     22.5     20.9     35.4      50.00   PATH
S_off[19]                 22.3     22.5     21.1     35.4      50.00   PATH
S_off[1]                  21.8     22.0     18.7     34.9      50.00   PATH
S_off[20]                 22.3     22.5     21.2     35.4      50.00   PATH
S_off[21]                 22.3     22.5     21.3     35.4      50.00   PATH
S_off[22]                 22.3     22.5     21.6     35.4      50.00   PATH
S_off[23]                 22.3     22.5     22.2     35.4      50.00   PATH
S_off[24]                 22.3     22.5     21.9     35.4      50.00   PATH
S_off[25]                 22.3     22.5     21.8     35.4      50.00   PATH
S_off[2]                  21.8     22.0     19.0     34.9      50.00   PATH
S_off[3]                  21.9     22.0     18.9     34.9      50.00   PATH
S_off[4]                  21.9     22.1     19.2     35.0      50.00   PATH
S_off[5]                  22.0     22.2     19.3     35.1      50.00   PATH
S_off[6]                  22.0     22.2     19.4     35.1      50.00   PATH
S_off[7]                  22.0     22.2     19.5     35.1      50.00   PATH
S_off[8]                  22.0     22.2     19.6     35.1      50.00   PATH
S_off[9]                  22.1     22.3     20.1     35.2      50.00   PATH
 ********************************************************************************
              Genesil Version v8.0.2 -- Fri Jan 18 12:12:18 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
********************************************************************************
PATH DELAY MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                    Corner: GUARANTEED
  Junction Temperature:112 deg C      Voltage:4.50v
  External Clock: Clk
```

```
 Included setup files:
  #0  set_hot                (Setup/Hold time, Violations -- Ma>
-------------------------------------------------------------------------------

                                PATH DELAY (ns)
Source Object     Connector            (Ph1) Min      Max
   Dest. Object       Connector        (Ph2)    Min      Max

 _______________ _________________
 dag_ren_pad____ DAG_R_en________          ---      ---
    _____________ _________________
    rf_pad[0]_____ RF_______________         ---      ---  PATH
 _______________ _________________
 dag_ren_pad____ DAG_R_en________          ---      ---
    _____________ _________________
    rf_pad[25]____ RF_______________         ---      ---  PATH
 _______________ _________________
>_______________ _________________
    _____________ _________________
    _____________ _________________
 ******************************************************************************
              Genesil Version v8.0.2 -- Fri Jan 18 12:16:18 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
******************************************************************************
SETUP AND HOLD MODE
-------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: GUARANTEED
  Junction Temperature:75 degree C      Voltage:5.00v
  External Clock: Clk
 Included setup files: default setup file
-------------------------------------------------------------------------------
                       INPUT SETUP AND HOLD TIMES (ns)
Input                    Setup Time          Hold Time
                        Ph1(f)   Ph2(f)     Ph1(f)   Ph2(f)
Booting                   ---     21.8        ---     -9.1       PATH
DAG_R_en                  ---      ---        ---      ---       PATH
Flush                     ---     34.9        ---     -1.0       PATH
Freeze                    ---     37.1        ---     -4.5       PATH
Guard                     ---     12.9        ---     -7.9       PATH
Ids_eq_ods_1              ---     11.1        ---     -8.5       PATH
Ids_eq_ods_2              ---     10.7        ---     -8.2       PATH
Ids_freeze                ---      3.7        ---     -1.3       PATH
Inst_en                   ---      4.7        ---     -2.0       PATH
Inst_rd                   ---     12.6        ---     -6.6       PATH
Kernel_mode               ---     48.2        ---     -3.9       PATH
N_reset                   ---     37.4        ---     -3.0       PATH
Ods_freeze                3.6      ---       -1.1      ---       PATH
Pc[0]                     ---     20.2        ---     -3.8       PATH
Pc[1]                     ---     20.4        ---     -3.9       PATH
Pc[2]                     ---     21.7        ---     -3.9       PATH
Pc[3]                     ---     20.8        ---     -5.6       PATH
RF[0]                     3.6      4.9       -2.8     -3.8       PATH
RF[10]                    2.5      3.8       -1.6     -2.6       PATH
RF[11]                    2.5      3.8       -1.6     -2.6       PATH
RF[12]                    2.4      3.6       -1.4     -2.4       PATH
RF[13]                    2.3      3.6       -1.4     -2.4       PATH
RF[14]                    2.3      3.6       -1.3     -2.4       PATH
RF[15]                    2.2      3.5       -1.3     -2.3       PATH
RF[16]                    2.2      3.5       -1.3     -2.3       PATH
RF[17]                    2.2      3.5       -1.2     -2.2       PATH
RF[18]                    2.1      3.4       -1.1     -2.1       PATH
RF[19]                    2.9      4.2       -2.0     -3.0       PATH
RF[1]                     2.9      4.2       -2.1     -3.1       PATH
RF[20]                    2.8      4.1       -1.9     -2.9       PATH
```

RF[21]	2.4	3.7	-1.5	-2.5	PATH
RF[22]	2.3	3.6	-1.4	-2.4	PATH
RF[23]	2.7	4.0	-1.8	-2.8	PATH
RF[24]	2.3	3.6	-1.4	-2.4	PATH
RF[25]	2.2	3.5	-1.2	-2.3	PATH
RF[26]	2.1	3.4	-1.1	-2.1	PATH
RF[27]	2.1	3.4	-1.2	-2.2	PATH
RF[28]	1.8	3.0	-0.8	-1.8	PATH
RF[29]	0.7	2.0	0.4	-0.6	PATH
RF[2]	2.9	4.2	-2.0	-3.0	PATH
RF[30]	---	---	---	---	PATH
RF[31]	---	---	---	---	PATH
RF[3]	2.9	4.2	-2.0	-3.0	PATH
RF[4]	2.8	4.1	-1.9	-2.9	PATH
RF[5]	2.8	4.1	-1.9	-2.9	PATH
RF[6]	2.7	4.0	-1.8	-2.8	PATH
RF[7]	3.1	4.4	-2.2	-3.3	PATH
RF[8]	3.0	4.3	-2.2	-3.2	PATH
RF[9]	2.6	3.9	-1.7	-2.7	PATH
RF_adr_mode[0]	9.3	9.9	-4.1	-5.4	PATH
RF_adr_mode[1]	8.3	8.9	-3.2	-4.4	PATH
RF_adr_mode[2]	6.3	7.1	-3.1	-4.5	PATH
RF_adr_mode[3]	6.5	7.3	-3.1	-4.7	PATH
RF_off[0]	7.1	8.8	-6.2	-5.0	PATH
RF_off[10]	7.1	8.7	-6.1	-4.6	PATH
RF_off[11]	6.9	8.6	-6.0	-4.5	PATH
RF_off[12]	6.9	8.5	-5.9	-4.4	PATH
RF_off[13]	6.9	8.5	-5.9	-4.4	PATH
RF_off[14]	6.9	8.6	-5.9	-4.5	PATH
RF_off[15]	6.9	8.6	-6.0	-4.5	PATH
RF_off[16]	6.9	8.6	-6.0	-4.5	PATH
RF_off[17]	7.0	8.7	-6.0	-4.6	PATH
RF_off[18]	7.0	8.7	-6.0	-4.7	PATH
RF_off[19]	7.5	9.1	-6.5	-5.1	PATH
RF_off[1]	7.1	8.8	-6.2	-5.0	PATH
RF_off[20]	7.5	9.2	-6.5	-5.1	PATH
RF_off[21]	7.6	9.3	-6.6	-5.2	PATH
RF_off[22]	7.7	9.3	-6.7	-5.2	PATH
RF_off[23]	7.7	9.4	-6.7	-5.3	PATH
RF_off[24]	7.8	9.4	-6.8	-5.4	PATH
RF_off[25]	7.8	9.5	-6.8	-5.5	PATH
RF_off[2]	7.8	9.4	-6.8	-5.4	PATH
RF_off[3]	7.8	9.4	-6.8	-5.4	PATH
RF_off[4]	7.7	9.3	-6.7	-5.3	PATH
RF_off[5]	7.6	9.2	-6.6	-5.2	PATH
RF_off[6]	7.5	9.2	-6.5	-5.1	PATH
RF_off[7]	7.4	9.0	-6.4	-5.0	PATH
RF_off[8]	6.9	8.5	-5.9	-4.4	PATH
RF_off[9]	7.2	8.9	-6.2	-4.8	PATH
S_adr_mode[0]	---	10.2	---	-5.1	PATH
S_adr_mode[1]	---	10.1	---	-5.0	PATH
S_adr_mode[2]	---	8.0	---	-4.9	PATH
S_adr_mode[3]	---	8.1	---	-5.1	PATH
S_off[0]	---	5.3	---	-3.4	PATH
S_off[10]	---	5.7	---	-3.7	PATH
S_off[11]	---	5.8	---	-3.8	PATH
S_off[12]	---	5.8	---	-3.9	PATH
S_off[13]	---	5.9	---	-3.9	PATH
S_off[14]	---	6.0	---	-4.0	PATH
S_off[15]	---	6.0	---	-4.1	PATH
S_off[16]	---	6.1	---	-4.2	PATH
S_off[17]	---	6.3	---	-4.3	PATH

```
S_off[18]                  ---      6.5         ---      -4.5       PATH
S_off[19]                  ---      6.5         ---      -4.6       PATH
S_off[1]                   ---      5.3         ---      -3.4       PATH
S_off[20]                  ---      6.6         ---      -4.7       PATH
S_off[21]                  ---      6.7         ---      -4.7       PATH
S_off[22]                  ---      6.7         ---      -4.8       PATH
S_off[23]                  ---      6.9         ---      -5.0       PATH
S_off[24]                  ---      7.0         ---      -5.0       PATH
S_off[25]                  ---      6.9         ---      -5.0       PATH
S_off[2]                   ---      5.3         ---      -3.4       PATH
S_off[3]                   ---      5.3         ---      -3.4       PATH
S_off[4]                   ---      5.4         ---      -3.4       PATH
S_off[5]                   ---      5.4         ---      -3.4       PATH
S_off[6]                   ---      5.4         ---      -3.4       PATH
S_off[7]                   ---      5.4         ---      -3.5       PATH
S_off[8]                   ---      5.5         ---      -3.5       PATH
S_off[9]                   ---      5.5         ---      -3.5       PATH
Valid_intr                 ---     31.8         ---      -2.6       PATH
 ********************************************************************************
             Genesil Version v8.0.2 -- Fri Jan 18 12:16:24 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
********************************************************************************
VIOLATION MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: GUARANTEED
  Junction Temperature:75 degree C      Voltage:5.00v
  External Clock: Clk
 Included setup files: default setup file
--------------------------------------------------------------------------------
                                NO VIOLATIONS
  Hold time check margin: 2.0ns
```

13.3. GUARANTEED, Room T, 5.0 V

```
 ********************************************************************************
             Genesil Version v8.0.2 -- Fri Jan 18 12:19:19 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
********************************************************************************
CLOCK REPORT MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: GUARANTEED
  Junction Temperature:62 deg C         Voltage:5.00v
  External Clock: Clk
 Included setup files:
  #0  cl_out_room            (Clock time, output delay -- Room >
--------------------------------------------------------------------------------
                            CLOCK TIMES (minimum)
Phase 1 High:    49.0   ns             Phase 2 High:    57.3   ns
            ----------                              ----------
Cycle (from Ph1):    99.2   ns        Cycle (from Ph2):   106.4   ns
                  ----------                              ----------
Minimum Cycle Time:   106.4   ns      Symmetric Cycle Time:    114.5   ns
                     ----------                              ----------
--------------------------------------------------------------------------------
                            CLOCK WORST CASE PATHS
Minimum Phase 1 high time is    49.0   ns set by:
                            ----------
  ** Clock delay: 3.5ns (52.6-49.0)
   Node                            Cumulative Delay      Transition
   <dr_gen/critical_rl/(internal)      52.6                 rise
```

```
   f_adr_gen/critical_rl/mnz          50.5              fall
   <en/critical_rl/f_boot_mode[0]     48.9              rise
   <n/critical_rl/f_boot_mode[0]'     48.0              rise
   <adr_gen/critical_rl/n_mode[0]     47.5              fall
   <en/critical_rl/rf_adr_mode[0]     47.1              rise
   rf_mode_pad[0]/rf_adr_mode         46.7              rise
   rf_mode_pad[0]/rf_adr_mode'        43.0              rise
   RF_adr_mode[0]                     40.0              rise


Minimum Phase 2 high time is    57.3   ns set by:
                           ----------
  ** Clock delay: 3.3ns (60.6-57.3)
   Node                           Cumulative Delay      Transition
   <ptr_mod/adr_ptr_dp/(internal)     60.6              rise
   <_mod/adr_ptr_dp/INTER4_ST1[4]     56.3              fall
   <tr_mod/adr_ptr_dp/adr_ptr_sel     51.9              fall
   <_mod/adr_ptr_ctrl/adr_ptr_sel     51.9              fall
   <mod/adr_ptr_ctrl/adr_ptr_sel'     50.2              fall
   <tr_mod/adr_ptr_ctrl/decrement     48.8              fall
   <r_mod/adr_ptr_ctrl/decrement'     46.5              fall
   <_ptr_mod/adr_ptr_ctrl/dec_mux     44.9              fall
   <ptr_mod/adr_ptr_ctrl/dec_mux'     44.8              fall
   <r_mod/adr_ptr_ctrl/decr_ap_in     43.2              fall
   <_mod/adr_ptr_ctrl/decr_ap_in'     42.7              fall
   <_mod/adr_ptr_ctrl/n_res_fl_fr     41.2              fall
   <mod/adr_ptr_ctrl/n_res_fl_fr'     41.1              fall
   <r_ptr_mod/adr_ptr_ctrl/freeze     39.3              rise
   <mod/adr_ptr_ctrl/n_freeze_buf     38.6              fall
   <od/adr_ptr_ctrl/n_freeze_buf'     38.4              fall
   <ptr_mod/adr_ptr_ctrl/n_freeze     37.2              fall
   freeze_pad/n_freeze                33.6              fall
   freeze_pad/n_freeze'               28.9              fall
   Freeze                             26.7              rise


Minimum cycle time (from Ph1) is   99.2    ns set by:
                              ----------
  ** Clock delay: 5.6ns (104.9-99.2)
   Node                           Cumulative Delay      Transition
   <toZ5fnowZ2eresetZ5fsigZ5b0Z5d    104.9              fall
   <gen/super_ctrl/GB.LP.NNZ5fN49    104.5              rise
   <.NNflagsZ2ftoZ5fnowZ2esetZ5fy    103.6              fall
   *<en/super_ctrl/GB.LP.NNZ5fN45    101.3              fall
   <_gen/super_ctrl/GB.LP.NNZ5fN2    100.9              rise
   <dr_gen/super_ctrl/n_adr_under    100.2              fall
   f_adr_gen/super_dp/n_adr_under    100.1              fall
   <adr_gen/super_dp/n_adr_under'     99.0              fall
   f_adr_gen/super_dp/adr[2]          73.9              fall
   f_adr_gen/super_dp/adr[2]'         73.2              fall
   <r_gen/super_dp/ea_tpap_OUT[2]     69.8              fall
   <adr_gen/super_dp/no_tp_ST2[1]     63.8              fall
   <_gen/super_dp/eff_adr1_OUT[1]     62.5              fall
   <_gen/super_dp/eff_adr1_IN1[0]     56.7              fall
   <dr_gen/super_dp/mode_not_zero     53.3              fall
   <gen/critical_rl/mode_not_zero     53.3              fall
   <en/critical_rl/mode_not_zero'     52.9              fall
   f_adr_gen/critical_rl/mnz          50.5              fall
   <en/critical_rl/f_boot_mode[0]     48.9              rise
   <n/critical_rl/f_boot_mode[0]'     48.0              rise
   <adr_gen/critical_rl/n_mode[0]     47.5              fall
   <en/critical_rl/rf_adr_mode[0]     47.1              rise
   rf_mode_pad[0]/rf_adr_mode         46.7              rise
```

```
   rf_mode_pad[0]/rf_adr_mode'          43.0                rise
   RF_adr_mode[0]                       40.0                rise

Minimum cycle time (from Ph2) is  106.4    ns set by:
                                  ----------
  ** Clock delay: 5.2ns (111.6-106.4)
   Node                              Cumulative Delay      Transition
   error_mod/error_ff/s_eq_f_2          111.6                rise
   odc_rf_mod/odc_mux/odc_out[1]        111.5                rise
   odc_rf_mod/odc_mux/odc_out[1]'       110.4                rise
   <_rf_mod/odc_mux/INTER0_ST1[1]       107.7                rise
   odc_rf_mod/odc_mux/odc_in[1]         106.3                rise
   odc_rf_mod/odc_ctrl/s2               106.2                rise
   odc_rf_mod/odc_ctrl/s2'              105.3                rise
   <rf_mod/odc_ctrl/GB.LP.NNZ5fN2       105.0                fall
   odc_rf_mod/odc_ctrl/s2_int           104.6                rise
   odc_rf_mod/odc_rf_dp/s_eq_f_2        104.6                rise
   odc_rf_mod/odc_rf_dp/s_eq_f_2'       104.1                rise
   odc_rf_mod/odc_rf_dp/s_adr[25]       100.3                rise
   s_adr_gen/super_dp/adr[25]            99.8                rise
   s_adr_gen/super_dp/adr[25]'           99.2                rise
   <_gen/super_dp/ea_tpap_OUT[25]        96.0                rise
   <r_gen/super_dp/bring_b_ST1[0]        69.6                fall
   s_adr_gen/super_dp/adr_ptr[0]         67.7                fall
   <ptr_mod/adr_ptr_dp/adr_ptr[0]        67.2                fall
   <tr_mod/adr_ptr_dp/adr_ptr[0]'        64.8                fall
   <mod/adr_ptr_dp/INTER5_VAL1[0]        63.1                fall
   *<tr_mod/adr_ptr_dp/(internal)        60.9                fall
   <_mod/adr_ptr_dp/INTER4_ST1[0]        56.3                fall
   <tr_mod/adr_ptr_dp/adr_ptr_sel        51.9                fall
   <_mod/adr_ptr_ctrl/adr_ptr_sel        51.9                fall
   <mod/adr_ptr_ctrl/adr_ptr_sel'        50.2                fall
   <tr_mod/adr_ptr_ctrl/decrement        48.8                fall
   <r_mod/adr_ptr_ctrl/decrement'        46.5                fall
   <_ptr_mod/adr_ptr_ctrl/dec_mux        44.9                fall
   <ptr_mod/adr_ptr_ctrl/dec_mux'        44.8                fall
   <r_mod/adr_ptr_ctrl/decr_ap_in        43.2                fall
   <_mod/adr_ptr_ctrl/decr_ap_in'        42.7                fall
   <_mod/adr_ptr_ctrl/n_res_fl_fr        41.2                fall
   <mod/adr_ptr_ctrl/n_res_fl_fr'        41.1                fall
   <r_ptr_mod/adr_ptr_ctrl/freeze        39.3                rise
   <mod/adr_ptr_ctrl/n_freeze_buf        38.6                fall
   <od/adr_ptr_ctrl/n_freeze_buf'        38.4                fall
   <ptr_mod/adr_ptr_ctrl/n_freeze        37.2                fall
   freeze_pad/n_freeze                   33.6                fall
   freeze_pad/n_freeze'                  28.9                fall
   Freeze                                26.7                rise
-------------------------------------------------------------------------------
 *******************************************************************************
              Genesil Version v8.0.2 -- Fri Jan 18 12:19:22 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
*******************************************************************************
OUTPUT DELAY MODE
-------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: GUARANTEED
  Junction Temperature:62 deg C         Voltage:5.00v
  External Clock: Clk
 Included setup files:
  #0  cl_out_room             (Clock time, output delay -- Room >
-------------------------------------------------------------------------------
                                OUTPUT DELAYS (ns)
Output                        Ph1(r) Delay      Ph2(r) Delay      Loading(pf)
```

	Min	Max	Min	Max		
DAG_Error	24.6	27.9	---	---	50.00	PATH
RF[0]	21.4	74.3	41.9	42.1	50.00	PATH
RF[10]	20.4	74.2	41.8	42.0	50.00	PATH
RF[11]	20.3	74.3	42.0	42.1	50.00	PATH
RF[12]	20.4	74.3	42.0	42.1	50.00	PATH
RF[13]	22.6	74.3	42.0	42.1	50.00	PATH
RF[14]	22.6	74.4	42.0	42.2	50.00	PATH
RF[15]	22.6	74.4	42.0	42.2	50.00	PATH
RF[16]	22.7	74.4	42.1	42.2	50.00	PATH
RF[17]	23.3	74.4	42.1	42.2	50.00	PATH
RF[18]	24.2	74.4	42.1	42.2	50.00	PATH
RF[19]	24.1	74.5	42.1	42.3	50.00	PATH
RF[1]	21.1	74.2	41.9	42.0	50.00	PATH
RF[20]	24.5	74.5	42.2	42.3	50.00	PATH
RF[21]	24.4	74.5	42.2	42.3	50.00	PATH
RF[22]	22.8	74.5	42.2	42.3	50.00	PATH
RF[23]	24.3	74.5	42.2	42.3	50.00	PATH
RF[24]	24.2	74.5	42.2	42.3	50.00	PATH
RF[25]	24.1	74.5	42.2	42.3	50.00	PATH
RF[26]	25.5	74.6	42.2	42.4	50.00	PATH
RF[27]	25.3	74.6	42.2	42.4	50.00	PATH
RF[28]	25.3	74.6	42.2	42.4	50.00	PATH
RF[29]	25.2	74.6	42.2	42.4	50.00	PATH
RF[2]	21.0	74.2	41.9	42.0	50.00	PATH
RF[30]	74.6	74.6	42.4	42.4	50.00	PATH
RF[31]	74.6	74.6	42.4	42.4	50.00	PATH
RF[3]	21.0	74.2	41.9	42.0	50.00	PATH
RF[4]	20.7	74.2	41.9	42.0	50.00	PATH
RF[5]	20.5	74.2	41.9	42.0	50.00	PATH
RF[6]	20.4	74.2	41.8	42.0	50.00	PATH
RF[7]	20.5	74.2	41.8	42.0	50.00	PATH
RF[8]	21.1	74.2	41.8	42.0	50.00	PATH
RF[9]	20.4	74.2	41.8	42.0	50.00	PATH
RF_adr[0]	18.9	53.8	20.9	22.0	50.00	PATH
RF_adr[10]	19.2	54.0	21.1	22.3	50.00	PATH
RF_adr[11]	19.2	54.1	21.2	22.3	50.00	PATH
RF_adr[12]	19.2	54.0	21.2	22.3	50.00	PATH
RF_adr[13]	19.2	54.0	21.2	22.3	50.00	PATH
RF_adr[14]	19.2	54.1	21.2	22.3	50.00	PATH
RF_adr[15]	19.3	54.1	21.2	22.4	50.00	PATH
RF_adr[16]	19.3	54.2	21.3	22.4	50.00	PATH
RF_adr[17]	19.4	55.0	21.3	22.4	50.00	PATH
RF_adr[18]	19.3	55.9	21.3	22.4	50.00	PATH
RF_adr[19]	19.4	56.8	21.3	22.5	50.00	PATH
RF_adr[1]	18.9	53.8	20.9	22.1	50.00	PATH
RF_adr[20]	19.5	57.8	21.5	22.6	50.00	PATH
RF_adr[21]	19.6	58.7	21.6	22.7	50.00	PATH
RF_adr[22]	19.7	59.7	21.6	22.7	50.00	PATH
RF_adr[23]	19.8	60.6	21.8	22.8	50.00	PATH
RF_adr[24]	19.8	61.6	21.8	22.8	50.00	PATH
RF_adr[25]	19.8	62.4	21.8	22.8	50.00	PATH
RF_adr[2]	18.9	53.8	20.9	22.1	50.00	PATH
RF_adr[3]	19.0	53.9	21.0	22.1	50.00	PATH
RF_adr[4]	19.1	53.9	21.0	22.2	50.00	PATH
RF_adr[5]	19.1	54.0	21.0	22.2	50.00	PATH
RF_adr[6]	19.1	54.0	21.1	22.2	50.00	PATH
RF_adr[7]	19.2	54.0	21.1	22.3	50.00	PATH
RF_adr[8]	19.2	54.1	21.2	22.3	50.00	PATH
RF_adr[9]	19.2	54.0	21.1	22.3	50.00	PATH
RF_adr_mode[0]	15.1	15.2	14.7	28.1	50.00	PATH
RF_adr_mode[1]	15.1	15.2	14.6	28.1	50.00	PATH

RF_adr_mode[2]	15.1	15.2	14.6	28.1	50.00	PATH
RF_adr_mode[3]	15.1	15.2	14.4	28.1	50.00	PATH
RF_off[0]	17.5	17.7	14.7	30.6	50.00	PATH
RF_off[10]	17.4	17.6	15.1	30.5	50.00	PATH
RF_off[11]	17.4	17.5	15.2	30.4	50.00	PATH
RF_off[12]	17.4	17.5	15.2	30.4	50.00	PATH
RF_off[13]	17.4	17.5	15.2	30.4	50.00	PATH
RF_off[14]	17.4	17.5	15.3	30.4	50.00	PATH
RF_off[15]	17.3	17.5	15.3	30.4	50.00	PATH
RF_off[16]	17.3	17.5	15.3	30.4	50.00	PATH
RF_off[17]	17.3	17.4	14.9	30.3	50.00	PATH
RF_off[18]	17.2	17.4	14.9	30.3	50.00	PATH
RF_off[19]	17.3	17.4	15.0	30.3	50.00	PATH
RF_off[1]	17.5	17.7	14.6	30.6	50.00	PATH
RF_off[20]	17.3	17.4	15.3	30.3	50.00	PATH
RF_off[21]	17.3	17.4	15.1	30.3	50.00	PATH
RF_off[22]	17.3	17.4	15.2	30.3	50.00	PATH
RF_off[23]	17.3	17.4	15.1	30.3	50.00	PATH
RF_off[24]	17.3	17.4	15.1	30.3	50.00	PATH
RF_off[25]	17.3	17.4	15.2	30.3	50.00	PATH
RF_off[2]	17.5	17.7	14.5	30.6	50.00	PATH
RF_off[3]	17.5	17.7	14.6	30.6	50.00	PATH
RF_off[4]	17.5	17.6	14.8	30.5	50.00	PATH
RF_off[5]	17.5	17.6	14.8	30.5	50.00	PATH
RF_off[6]	17.5	17.6	14.9	30.5	50.00	PATH
RF_off[7]	17.5	17.6	14.9	30.5	50.00	PATH
RF_off[8]	17.4	17.6	15.0	30.5	50.00	PATH
RF_off[9]	17.4	17.6	15.0	30.5	50.00	PATH
R_eq_f_1	18.3	66.5	---	---	50.00	PATH
R_eq_f_2	18.1	66.7	---	---	50.00	PATH
SF_adr[0]	18.8	55.1	20.8	22.7	50.00	PATH
SF_adr[10]	19.3	55.4	21.3	23.1	50.00	PATH
SF_adr[11]	19.4	55.5	21.3	23.2	50.00	PATH
SF_adr[12]	19.5	55.5	21.4	23.3	50.00	PATH
SF_adr[13]	19.5	55.6	21.5	23.3	50.00	PATH
SF_adr[14]	19.6	55.6	21.5	23.4	50.00	PATH
SF_adr[15]	19.7	55.7	21.7	23.5	50.00	PATH
SF_adr[16]	19.7	55.7	21.7	23.5	50.00	PATH
SF_adr[17]	19.9	56.6	21.8	23.6	50.00	PATH
SF_adr[18]	19.9	57.6	21.9	23.7	50.00	PATH
SF_adr[19]	20.0	58.5	22.0	23.7	50.00	PATH
SF_adr[1]	18.8	55.0	20.7	22.7	50.00	PATH
SF_adr[20]	20.1	59.5	22.0	23.8	50.00	PATH
SF_adr[21]	20.1	60.4	22.1	23.8	50.00	PATH
SF_adr[22]	20.2	61.4	22.1	23.9	50.00	PATH
SF_adr[23]	20.2	62.3	22.2	23.9	50.00	PATH
SF_adr[24]	20.3	63.2	22.3	24.0	50.00	PATH
SF_adr[25]	20.5	64.2	22.4	24.1	50.00	PATH
SF_adr[2]	18.8	55.0	20.8	22.7	50.00	PATH
SF_adr[3]	18.9	55.1	20.8	22.8	50.00	PATH
SF_adr[4]	18.9	55.1	20.9	22.8	50.00	PATH
SF_adr[5]	19.0	55.2	20.9	22.9	50.00	PATH
SF_adr[6]	19.0	55.2	21.0	22.9	50.00	PATH
SF_adr[7]	19.1	55.2	21.1	23.0	50.00	PATH
SF_adr[8]	19.2	55.4	21.2	23.1	50.00	PATH
SF_adr[9]	19.3	55.4	21.3	23.1	50.00	PATH
S_adr_mode[0]	15.5	15.6	19.1	28.5	50.00	PATH
S_adr_mode[1]	15.5	15.6	19.1	28.5	50.00	PATH
S_adr_mode[2]	15.5	15.6	18.9	28.5	50.00	PATH
S_adr_mode[3]	15.5	15.6	18.8	28.5	50.00	PATH
S_eq_f_1	18.8	67.5	---	---	50.00	PATH
S_eq_f_2	18.6	67.5	---	---	50.00	PATH

```
S_off[0]                  17.4     17.6     15.0     30.5      50.00   PATH
S_off[10]                 17.7     17.9     16.1     30.8      50.00   PATH
S_off[11]                 17.7     17.9     16.2     30.8      50.00   PATH
S_off[12]                 17.8     17.9     16.2     30.8      50.00   PATH
S_off[13]                 17.8     17.9     16.3     30.8      50.00   PATH
S_off[14]                 17.8     17.9     16.4     30.8      50.00   PATH
S_off[15]                 17.8     17.9     16.6     30.9      50.00   PATH
S_off[16]                 17.8     18.0     16.7     30.9      50.00   PATH
S_off[17]                 17.8     18.0     16.7     30.9      50.00   PATH
S_off[18]                 17.9     18.0     16.8     30.9      50.00   PATH
S_off[19]                 17.9     18.0     17.0     30.9      50.00   PATH
S_off[1]                  17.5     17.6     15.0     30.5      50.00   PATH
S_off[20]                 17.9     18.0     17.0     30.9      50.00   PATH
S_off[21]                 17.9     18.0     17.1     30.9      50.00   PATH
S_off[22]                 17.9     18.0     17.3     30.9      50.00   PATH
S_off[23]                 17.9     18.0     17.8     30.9      50.00   PATH
S_off[24]                 17.9     18.0     17.5     30.9      50.00   PATH
S_off[25]                 17.9     18.0     17.5     30.9      50.00   PATH
S_off[2]                  17.5     17.6     15.3     30.5      50.00   PATH
S_off[3]                  17.5     17.7     15.2     30.6      50.00   PATH
S_off[4]                  17.6     17.7     15.4     30.6      50.00   PATH
S_off[5]                  17.6     17.8     15.5     30.7      50.00   PATH
S_off[6]                  17.6     17.8     15.6     30.7      50.00   PATH
S_off[7]                  17.7     17.8     15.7     30.7      50.00   PATH
S_off[8]                  17.7     17.8     15.7     30.7      50.00   PATH
S_off[9]                  17.7     17.9     16.1     30.8      50.00   PATH
 ********************************************************************************
             Genesil Version v8.0.2 -- Fri Jan 18 12:19:53 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
********************************************************************************
PATH DELAY MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: GUARANTEED
  Junction Temperature:62 deg C         Voltage:5.00v
  External Clock: Clk
 Included setup files:
  #0  cl_out_room             (Clock time, output delay -- Room >
--------------------------------------------------------------------------------
                              PATH DELAY (ns)
Source Object     Connector           (Ph1) Min       Max
   Dest. Object       Connector       (Ph2)    Min       Max

 _____________ _________________
 dag_ren_pad____ DAG_R_en________          ---       ---

    _____________ _________________
    rf_pad[0]_____ RF_______________        ---       ---  PATH

 _____________ _________________
 dag_ren_pad____ DAG_R_en________          ---       ---

    _____________ _________________
    rf_pad[25]____ RF_______________        ---       ---  PATH

 _____________ _________________
>_____________ _________________

    _____________ _________________
    _____________ _________________
 ********************************************************************************
             Genesil Version v8.0.2 -- Fri Jan 18 12:26:01 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
********************************************************************************
SETUP AND HOLD MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: GUARANTEED
  Junction Temperature:62 deg C         Voltage:5.00v
  External Clock: Clk
```

```
 Included setup files:
  #0  set_room                (Setup/Hold time, Violations -- Ro>
```

Input	INPUT SETUP AND HOLD TIMES (ns) Setup Time Ph1(f)	Setup Time Ph2(f)	Hold Time Ph1(f)	Hold Time Ph2(f)	
Booting	---	---	---	---	PATH
DAG_R_en	---	---	---	---	PATH
Flush	---	---	---	---	PATH
Freeze	---	35.8	---	-4.3	PATH
Guard	---	12.4	---	-7.6	PATH
Ids_eq_ods_1	---	---	---	---	PATH
Ids_eq_ods_2	---	---	---	---	PATH
Ids_freeze	---	3.6	---	-1.3	PATH
Inst_en	---	4.5	---	-1.9	PATH
Inst_rd	---	12.2	---	-6.4	PATH
Kernel_mode	---	---	---	---	PATH
N_reset	---	---	---	---	PATH
Ods_freeze	3.4	---	-1.1	---	PATH
Pc[0]	---	19.5	---	-3.6	PATH
Pc[1]	---	19.7	---	-3.8	PATH
Pc[2]	---	20.9	---	-3.8	PATH
Pc[3]	---	20.1	---	-5.4	PATH
RF[0]	3.5	4.7	-2.7	-3.6	PATH
RF[10]	2.4	3.7	-1.6	-2.6	PATH
RF[11]	2.4	3.7	-1.6	-2.5	PATH
RF[12]	2.3	3.5	-1.4	-2.4	PATH
RF[13]	2.2	3.5	-1.3	-2.3	PATH
RF[14]	2.2	3.4	-1.3	-2.3	PATH
RF[15]	2.1	3.4	-1.3	-2.2	PATH
RF[16]	2.1	3.4	-1.2	-2.2	PATH
RF[17]	2.1	3.3	-1.2	-2.2	PATH
RF[18]	2.0	3.3	-1.1	-2.1	PATH
RF[19]	2.8	4.0	-1.9	-2.9	PATH
RF[1]	2.8	4.1	-2.0	-3.0	PATH
RF[20]	2.7	4.0	-1.9	-2.8	PATH
RF[21]	2.3	3.6	-1.5	-2.5	PATH
RF[22]	2.2	3.5	-1.3	-2.3	PATH
RF[23]	2.6	3.9	-1.7	-2.7	PATH
RF[24]	2.2	3.5	-1.4	-2.3	PATH
RF[25]	2.1	3.4	-1.2	-2.2	PATH
RF[26]	2.0	3.3	-1.1	-2.1	PATH
RF[27]	2.0	3.3	-1.1	-2.1	PATH
RF[28]	1.7	2.9	-0.7	-1.7	PATH
RF[29]	0.7	1.9	0.4	-0.6	PATH
RF[2]	2.8	4.0	-1.9	-2.9	PATH
RF[30]	---	---	---	---	PATH
RF[31]	---	---	---	---	PATH
RF[3]	2.8	4.0	-1.9	-2.9	PATH
RF[4]	2.7	4.0	-1.8	-2.8	PATH
RF[5]	2.7	3.9	-1.8	-2.8	PATH
RF[6]	2.6	3.9	-1.8	-2.8	PATH
RF[7]	3.0	4.3	-2.2	-3.1	PATH
RF[8]	2.9	4.2	-2.1	-3.1	PATH
RF[9]	2.5	3.7	-1.6	-2.6	PATH
RF_adr_mode[0]	9.0	9.6	-4.0	-5.2	PATH
RF_adr_mode[1]	8.0	8.6	-3.0	-4.3	PATH
RF_adr_mode[2]	6.1	6.9	-2.9	-4.4	PATH
RF_adr_mode[3]	6.2	7.0	-3.0	-4.5	PATH
RF_off[0]	6.9	8.5	-5.9	-4.8	PATH
RF_off[10]	6.8	8.4	-5.9	-4.5	PATH
RF_off[11]	6.7	8.3	-5.7	-4.3	PATH

```
RF_off[12]              6.6      8.2       -5.7      -4.3      PATH
RF_off[13]              6.7      8.3       -5.7      -4.3      PATH
RF_off[14]              6.7      8.3       -5.7      -4.3      PATH
RF_off[15]              6.7      8.3       -5.7      -4.3      PATH
RF_off[16]              6.7      8.3       -5.8      -4.4      PATH
RF_off[17]              6.8      8.4       -5.8      -4.5      PATH
RF_off[18]              6.8      8.4       -5.8      -4.5      PATH
RF_off[19]              7.2      8.8       -6.3      -4.9      PATH
RF_off[1]               6.9      8.5       -5.9      -4.8      PATH
RF_off[20]              7.3      8.9       -6.3      -5.0      PATH
RF_off[21]              7.3      8.9       -6.4      -5.0      PATH
RF_off[22]              7.4      9.0       -6.4      -5.1      PATH
RF_off[23]              7.5      9.1       -6.5      -5.1      PATH
RF_off[24]              7.5      9.1       -6.5      -5.2      PATH
RF_off[25]              7.5      9.1       -6.6      -5.3      PATH
RF_off[2]               7.5      9.1       -6.5      -5.2      PATH
RF_off[3]               7.5      9.1       -6.5      -5.2      PATH
RF_off[4]               7.4      9.0       -6.4      -5.1      PATH
RF_off[5]               7.3      8.9       -6.3      -5.0      PATH
RF_off[6]               7.2      8.8       -6.3      -5.0      PATH
RF_off[7]               7.1      8.7       -6.2      -4.8      PATH
RF_off[8]               6.6      8.2       -5.7      -4.3      PATH
RF_off[9]               7.0      8.6       -6.0      -4.6      PATH
S_adr_mode[0]           ---      9.8        ---      -4.9      PATH
S_adr_mode[1]           ---      9.8        ---      -4.8      PATH
S_adr_mode[2]           ---      7.7        ---      -4.7      PATH
S_adr_mode[3]           ---      7.8        ---      -4.9      PATH
S_off[0]                ---      5.1        ---      -3.3      PATH
S_off[10]               ---      5.5        ---      -3.6      PATH
S_off[11]               ---      5.6        ---      -3.7      PATH
S_off[12]               ---      5.6        ---      -3.8      PATH
S_off[13]               ---      5.7        ---      -3.8      PATH
S_off[14]               ---      5.8        ---      -3.9      PATH
S_off[15]               ---      5.8        ---      -4.0      PATH
S_off[16]               ---      5.9        ---      -4.0      PATH
S_off[17]               ---      6.1        ---      -4.2      PATH
S_off[18]               ---      6.2        ---      -4.4      PATH
S_off[19]               ---      6.3        ---      -4.4      PATH
S_off[1]                ---      5.1        ---      -3.3      PATH
S_off[20]               ---      6.4        ---      -4.5      PATH
S_off[21]               ---      6.4        ---      -4.6      PATH
S_off[22]               ---      6.5        ---      -4.6      PATH
S_off[23]               ---      6.6        ---      -4.8      PATH
S_off[24]               ---      6.7        ---      -4.9      PATH
S_off[25]               ---      6.7        ---      -4.8      PATH
S_off[2]                ---      5.1        ---      -3.3      PATH
S_off[3]                ---      5.1        ---      -3.3      PATH
S_off[4]                ---      5.2        ---      -3.3      PATH
S_off[5]                ---      5.2        ---      -3.3      PATH
S_off[6]                ---      5.2        ---      -3.3      PATH
S_off[7]                ---      5.2        ---      -3.3      PATH
S_off[8]                ---      5.3        ---      -3.4      PATH
S_off[9]                ---      5.3        ---      -3.4      PATH
Valid_intr              ---      ---        ---       ---      PATH
 ********************************************************************************
              Genesil Version v8.0.2 -- Fri Jan 18 12:26:07 1991
Chip: /tmp_mnt/net/yoda/mnta/iag/iag/gt_vic/dag                 Timing Analyzer
********************************************************************************
VIOLATION MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                    Corner: GUARANTEED
  Junction Temperature:62 deg C       Voltage:5.00v
```

```
 External Clock: Clk
Included setup files:
 #0  set_room                (Setup/Hold time, Violations -- Ro>
-------------------------------------------------------------------------------
                                NO VIOLATIONS
 Hold time check margin: 2.0ns
```

DV CHECKLIST

1. DV CONTROL NUMBER : _____

2. CUSTOMER INFORMATION

Customer Name : Georgia Tech / CERL Chip Name : GT–VDAG

Address : 400 Tenth Street FAX : (404) 894–3120

CRB Room 377

Atlanta, GA 30332–0540

Project Manager : Dr. C. O. Alford Phone : (404) 894–2505

Design Engineer : Samuel H. Russ Phone : (404) 894–7472

Toshiro Kubota Phone : (404) 894–2506

Dr. Wei Siong Tan Phone : (404) 894–2508

Test Engineer : Joseph I. Chamdani Phone : (404) 894–2527

3. SERVICES INFORMATION

xx Design Verification Service only. PO #_____

_____ Prototype Service and Design Verification. PO #_____

_____ 1.8% Maintenance

_____ SCS Test _____ Foundry Test _____ Customer Test

When DV is complete, send verified physical database tape to

Customer Y N Silicon Vendor Y N

4. DV CONTACT : Ying Chow Phone : (408) 371–2900

5. REGRESSION

5.1. GENESIL Version : 8.0.2

5.2. Name of Session Log from recompile : com_force_build.001

5.3. Include DV regression.CMD : DV_regression.001 (simulation and timing)

5.4. Size of database (MB): 110 Guess ___ Density : 6250 ___ 1600 ___ TK50 ___
Tar xx wbak ___ Apollo Cartridge ____
(compressed) Sun Cartridge xx

6. FUNCTIONAL INFORMATION (check when included)

6.1. Number of Transistors : xx

6.2. Key Parameters : xx Testing ____

6.3. DV pin description : xx Testing ____

6.4. Block Diagram : ____ Testing xx

6.5. Functional Description : ____ Testing xx

6.6. Timing Diagrams at Pins : ____ Testing xx

6.7. Annotated Views : ____ Testing xx Annotated Schematics : ____ Testing xx

6.8. Chip Text Specification on tape : xx Density: 6250____ 1600____ TK50_____
(dag_text_spec.012.Z) Apollo Cartridge_____
Sun Cartridge xx

7. PHYSICAL INFORMATION

7.1. Fabline Name : HP2_CN10B
Customer–Specific : Y N Fabline GENECAL Directory on tape : Y N
Fabline GENESIL Directory on tape : Y N
Fabline Calibration Status : Production : _____ Beta : _____ Alpha : xx
NOTE: If not a production fabline, then approval from SCS is required.

7.2. Plots: (check when included or indicate filename)
Chip Route (D size) : xx Bonding Diagram (B size) : xx
Route Filename : route_d.031 Bonding Filename : bond_b.031

7.3. Die Size : Reported Die Size : 414.8 x 409.5 square–mils
Maximum Acceptable Die Size (+/– 2%) : 450 x 450 square–mils
Minimum Acceptable Die Size (+/– 2%) : 280 x 280 square–mils

7.4. GENESIL Package Name : CPGA224f2 Spec included? Y N
Cavity/Well Size : 480 mils by 480 mils
Non–GENESIL Supplied Package? Y N Text Spec included on tape? Y N
Vendor Name/Part # : KYOCERA KD–P86077C Foundry Approval? Y N

7.5. External Block: none

7.6. LRAM: Y N LROM: Y N LPLA: Y N LogicCompiler Blocks: Y N

7.7. Test Pad (PM Pad) is included? Y N (Required for PS)

7.8. Power Pad : VCC: Core 4 VSS: Core 4
Ring 14 Ring 13

NP protection for nwell pad? Y N

TTL output pads or N Protection for inputs? Y N
If yes, have you received silicon vendor approval? Y N

Error in PADRING.033 (PADRING.DRC)? Y N Hardcopy attached? Y N

ESD requirements _____ Approved by SCS? Y N

8. ELECTRICAL INFORMATION

8.1. Chip Frequency Specified in netlist : 10.0 MHz Target frequency : 10.0 MHz
8.2. Power Dissipation: GENESIL = 0.946 W at 10 MHz Spec = 1.0 W at 10.0 MHz
8.3. Operating Voltage: from 4.5 Volts to 5.5 Volts

9. SIMULATION

9.1. Number of Clocking Regimes : 1

	Clock Pad Name	DIV/NO DIV	Ext Clock Name	Int PHASE A/PHASE B Name
1.	Clock_pad	NO_DIV	Clk	PHASE_A / PHASE_B
2.				
3.				
4.				
5.				

9.2. Simulation Setup Files:
Name : designinit.080 Listings attached : No
Description : default clock setup

Affected Tests : All

Name : _____ Listings attached : _____
Description : _____

Affected Tests : _____

Name : _____ Listings attached : _____
Description : _____

Affected Tests : _____

Name : _____ Listings attached : _____
Description : _____

Affected Tests : _____

9.3. Test Vector Set:
Total No. of Vectors : 36,223

NOTE : Test vectors written one phase per vector have a maximum test frequency on the IMS Tester of 10 MHz. Test vectors written one cycle per vector have a maximum test frequency on the IMS Tester of 20 MHz.

1. Name : vec1_trace.083 No of vectors : 6,133
   Description : test the loac and store operation

   Portions of Chip Tested : all

   Pass with GFL model? yes
   Pass with GSL model? yes Use for PS testing? Y N
   Pass Fight Test? yes

2. Name : vec2_trace.083 No of vectors : 7,433
   Description : continuation of vec1_trace

   Portions of Chip Tested : all

   Pass with GFL model? yes
   Pass with GSL model? yes Use for PS testing? Y N
   Pass Fight Test? yes

3. Name : vec3_trace.083 No of vectors : 3,719
   Description : continuation of vec1_trace

   Portions of Chip Tested : all

   Pass with GFL model? yes
   Pass with GSL model? yes Use for PS testing? Y N
   Pass Fight Test? yes

4. Name : vec4_trace.083 No of vectors : 5,979
   Description : continuation of vec1_trace

   Portions of Chip Tested : all

   Pass with GFL model? yes
   Pass with GSL model? yes Use for PS testing? Y N
   Pass Fight Test? yes

5. Name : vec5_trace.083 No of vectors : 4,609
Description : continuation of vec1_trace

Portions of Chip Tested :

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

6. Name : iosat_trace.083 No of vectors : 3,833
Description : created as part of multichip simulation involving GT–VIAG and GT–VFPU/1a

Portions of Chip Tested : all

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

7. Name : sort4_trace.083 No of vectors : 4,517
Description : same with iosat_trace.083

Portions of Chip Tested : all

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

8. Name : No of vectors :
Description :

Portions of Chip Tested :

Pass with GFL model?
Pass with GSL model? Use for PS testing? Y N
Pass Fight Test?

9. Name : _____ No of vectors : _____
Description : _____
_____
_____

Portions of Chip Tested : _____
_____

Pass with GFL model? _____
Pass with GSL model? _____ Use for PS testing? Y N
Pass Fight Test? _____

10. Name : _____ No of vectors : _____
Description : _____
_____
_____

Portions of Chip Tested : _____
_____

Pass with GFL model? _____
Pass with GSL model? _____ Use for PS testing? Y N
Pass Fight Test? _____

11. Name : _____ No of vectors : _____
Description : _____
_____
_____

Portions of Chip Tested : _____
_____

Pass with GFL model? _____
Pass with GSL model? _____ Use for PS testing? Y N
Pass Fight Test? _____

9.4. IMS Grouping within limitation? Y N (Required for PS only)
9.5. Tester clock frequency = 10.0 MHz
9.6. Signals that must be glitch free: Y N

	Signal Name	Ran GSL with glitch detection feature on?
1.	_____	Y N
2.	_____	Y N
3.	_____	Y N
4.	_____	Y N
5.	_____	Y N
6.	_____	Y N
7.	_____	Y N
8.	_____	Y N
9.	_____	Y N

10. TIMING ANALYSIS

10.1. System Environment

Temperature Coefficient: 35 Degrees C / Watt (theta JA)
Operating Temp : from 25 C (min) to 75 C (max)
Operating Voltage : from 4.5 V (min) to 5.5 V (max)
room junction temp = 25 + (theta JA * Power) = 61.5 degrees C
maximum junction temp = maximum ambient temp + (theta JA * Power) = 111.5 degrees C

10.2. Reports (Include the following reports)

(required for PS)* guaranteed corner 5.0V room junc temp	(required for PS)* guaranteed corner min operating V max junction temp	typical corner min operating V max junction temp
Cycle : xx	Cycle : xx	Cycle :
Setup/Hold : xx	Setup/Hold : xx	Setup/Hold :
Output Delay : xx	Output Delay : xx	Output Delay :
Violation : xx	Violation : xx	Violation :

10.3. Timing Setup Files:

Name : cl_out_room Listings attached : yes
Temperature : 62 degrees C Voltage : 5.00 V
Description : clock, output delay with room temprature and normal voltage

Name : cl_out_hot Listings attached : yes
Temperature : 112 degrees C Voltage : 4.50 V
Description : clock, output delay with maximum temprature and minimum voltage

Name : set_room Listings attached : yes
Temperature : 62 degrees C Voltage : 5.00V
Description : setup and hold time and violations at room temp and normal voltage

Name : set_hot Listings attached : yes
Temperature : 112 degrees C Voltage : 4.50V
Description : setup and hold time and violations at max temp and min voltage

Name : clock_output Listings attached : yes
Temperature : 75 degrees C Voltage : 5.00 V
Description : clock, output delay with room temprature and normal voltage
(used for TYPICAL analysis)

Name : setup hold Listings attached : yes
Temperature : 75 degrees C Voltage : 5.00V
Description : setup and hold time and violations at room temp and normal voltage
(used for TYPICAL analysis)

10.4. Critical Boundary Conditions:
List critical paths here or annotate the timing report.
Attach additional pages if needed.

Clock Name : Clk

	report	limit (+/–5%)	report	limit (+/–5%)
1. Phase 1 High	46.1 ns	50.0 ns		
2. Phase 2 High	46.6 ns	50.0 ns		
3. Symmetric Cycle	94.0 ns	100.0 ns		
4. Minimum Cycle	94.0 ns	100.0 ns		

Outputs

	Signal Name	load (pF)	delay	limit
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				

Inputs

	Signal Name	setup report / limit	hold report / limit
1.		/	/
2.		/	/
3.		/	/
4.		/	/
5.		/	/
6.		/	/
7.		/	/
8.		/	/
9.		/	/

10.5. Hold Time Violations : none (At 2.0 nsec.)

11. DC CHARACTERISTICS

PARA–METERS	DESCRIPTION	CONDITIONS 0 to 70	CONDITIONS –55 to +125	MIN	MAX
DATA PAD INPUT ONLY					
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IIL	Input Leakage	VSS<Vin<VDD	VSS<Vin<VDD	–10uA	10uA
CIN	Input Capacitance				6.0pf
DATA PAD OUTPUT ONLY					
VOH	Output High Voltage	VDD= 4.5V IOH=–2.2	VDD= 4.5V IOH=–2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
IOZ	Output Leakage current(high Z)	VSS<Vout<VDD	VSS<Vout<VDD	–10uA	10uA
COUT	Output Capacitance				7.0pf
DATA PAD INPUT/OUTPUT					
VOH	Output High Voltage	VDD= 4.5V IOH=–2.2	VDD= 4.5V IOH=–2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IOZ	Output leakage current (high Z)	VSS<Vout<VDD	VSS<Vout<VDD	–10uA	10uA
CIO	Input/Output Capacitance				7.0pf
CLOCK PAD					
VIH	Input High Voltage			3.9V	
VIL	Input Low Voltage				0.6V
IIL	Input Leakage	VSS<Vin<VDD	VSS<Vin<VDD	–10uA	10uA
CIN	Input Capacitance				15pf

NOTE: All parameters at a supply voltage of VDD = 5V (+/– 10%).

12. CUSTOMER COMMENTS

Pre–Verification Comments

1. tnet reports 6 "undriven nets". These are correct, and do not represent an actual error.

2. Genesil's Padring CCC flags bond angle, bond length, and wire crossing problems. A copy of the bonding diagram has been sent to HP for approval.

Post–Verification Comments

1. Power and ground routing forced re–placement of one datapath.

2. Die Size is now approximately 412.5 by 412.9 mils.

3. Timing Analysis revealed hold time violations in error_mod/error_ff. Spice analysis indicated that this would not be a problem.

4. Genesil flagged bonding angle, length, and wire crossing problems. HP as checked the bonding and found it acceptable for prototype purposes.

13. CUSTOMER APPROVAL

The undersigned understands that if any design changes are initiated by the Customer subsequent to this sign–off, the Customer is liable for any charges imposed by Silicon Compiler Systems as agreed to in either the Design Verification Terms & Conditions or the Prototype Services Terms & Conditions. In addition, such changes require the DV process to be started from the beginning, which results in extended DV schedules.

Customer Approval : _____ Date ___/__/_____

Title : _____

14. SCS APPROVAL

Pre–Verification Comments

_____

_____

_____

_____

SCS Approval : _____ Date ___/___/___
Regional Field Application Consultant

SCS Approval : _____ Date ___/___/___
Technical Support Team Leader